Tribologically-induced Damage in Cutting and Polishing of Silicon

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***Abstract*-This paper discusses the influence of tribology on the mechanical properties of cutting, shaping and forming silicon wafers. These processes, such as multi wire slurry sawing, diamond wire sawing, lapping and grinding, Chemical Mechanical Polishing (CMP), and dicing, utilize either a two-body or a three-body material removal, where the fundamental cutting process results from micro-fracturing of silicon by the hard abrasives. There are specific types of defects and related fracture strength characteristics for each process. The associated surface and subsurface damage, especially microcracks, have a dominant effect on the fracture strength of the silicon substrates, even playing a more significant role than edge chipping. There is a need to reduce the surface and subsurface damage, possibly through ductile regime machining/polishing, to improve the mechanical strength.**

Keywords- Fracture Strength; Defects; Microcracks; Silicon

I. INTRODUCTION

Tribological phenomena can be found in many semiconductor manufacturing processes, such as silicon wafering [1], CMP [2], dicing [3], milling [4], and others [5-6]. For example, multi-wire slurry sawing is based on a three-body material removal process involving hard abrasive SiC grits, steel wire, and silicon. In contrast, diamond wire sawing is a two-body material removal process, which comprises fixed diamond grits and silicon material. Similarly, grinding and lapping are based on a two-body process to affect fast material removal, while CMP is a three-body material removal process involving nano-sized particles to achieve improved planarity and surface finish. The application of hydrodynamic and elasto-hydrodynamic principles in selection of the cutting fluid is also important in these processes. These tribological processes have played a critical role in device technology development, and in low cost/high volume semiconductor manufacturing.

During material removal, the aforementioned tribological processes also introduce surface and subsurface damage that is detrimental to the material properties and/or performance. Defects in a semiconductor material can be generally categorized as point, line, area, and volume defects by their dimensions and from the viewpoint of electronic properties [7-8]. In terms of mechanical properties, the contribution of each type of defect is quite different. It is known that tribology-related defects that appear on the surfaces and edges of the semiconductor substrate will have a significant effect on the mechanical strength of silicon [9-12]. In this paper, we present some results of how defects associated with several semiconductor cutting and polishing processes influence the mechanical strength of silicon.

II. EXPERIMENTAL METHODS

Five different semiconductor processes were studied, including multi-wire slurry sawing, diamond wire sawing, lapping and grinding, CMP, and dicing. The former two are targeted for photovoltaic (PV) manufacturing, and the last three for integrated circuit (IC) applications. PV wafers described in this study are as-cut multicrystalline silicon wafers with a nominal thickness of 200 μm. Two wire sawing processes, multi-wire slurry sawing and diamond wire sawing, were compared. IC wafers are one-side polished CZ silicon with a nominal thickness of 550 μm. Lapping and grinding, and CMP processes are represented by the rough and smooth side of the IC wafers, respectively.

Mechanical strength was studied by performing four line bending tests on small rectangular bars that were cut from full-sized wafers. For IC wafers, tests are conducted either with the smooth surface downward (SSD) or rough surface downward (RSD) to maintain the measured surface of interest in the tensile loading zone. Since both sides of the PV wafers are similar, there is no particular orientation selection during testing.

Fracture strength of the tested silicon sample was calculated from linear elastic fracture mechanics as:

$$\sigma = \frac{3F\left(l_o - l_i\right)}{2bd^2} \tag{1}$$

where F is the applied load (resultant of the normal and tangential forces), b is the sample width, d is the wafer thickness, and l_o and l_i are the distances between the lower and upper loading beams, respectively.

A characteristic strength for each sample condition was calculated using Weibull statistics as:

$$p_f = 1 - \exp\left[-\left(\frac{\sigma}{\sigma_\theta}\right)^m\right] \quad (2)$$

where P_f is the probability of failure, σ is the fracture stress, σ_θ is the characteristic strength at which the probability of failure is 0.632, and m is the Weibull modulus.

In addition to surface defects, edge defects that are created by dicing were also studied. The one-side polished IC wafers were diced at various feed rates from 0.25 to 12.7 m/s to mimic different degrees of edge damage. The diced samples were bent with either the smooth surface downward (SSD) or rough surface upward (RSD) to measure the effect of edge defects on the overall fracture strength.

Surface morphology was characterized by a 3D laser confocal microscope and a scanning electron microscope (SEM). Surface and subsurface microracks were examined by SEM on the top surface and on bevel-polished samples.

III. RESULTS AND DISCUSSIONS

A. Effect of Surface Defects

Fig. 1 shows the Weibull plot of fracture strengths for five different surfaces. There is a clear difference in measured fracture strength among these wafers due to differences in their surface characteristics. The CMP polished surface shows the highest fracture strength. The maximum fracture strength for SSD case reaches about 720 MPa, and the characteristic strength is 469 MPa. On the other hand, the fracture strength of the same type of wafers bent in the rough surface downward (RSD) orientation is much lower, with a characteristic strength of only 205 MPa. It can be seen that the surface condition plays a critical role in the mechanical strength of silicon.

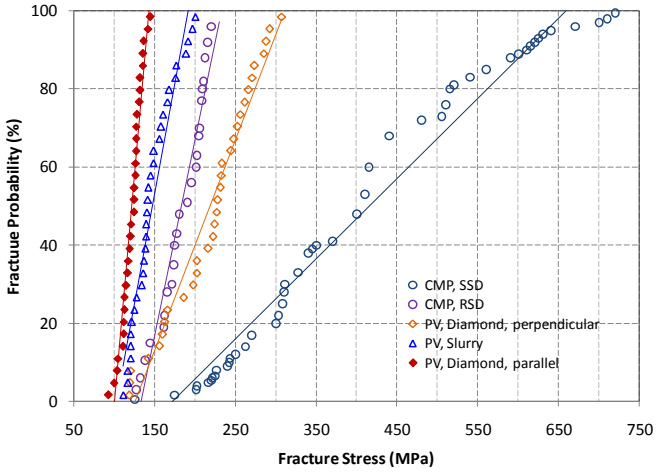

Fig. 1 Weibull plot of fracture strength distribution for various wafer surface conditions

The wire sawn PV wafers display a different characteristic from the IC wafers. There is a fracture strength anisotropy in the diamond wire sawn wafers: a relatively higher fracture strength is measured if bent perpendicular to the wire saw marks (Diamond, perpendicular) but a lower fracture strength if bent parallel to the saw marks (Diamond, parallel). The characteristic strengths are ~240 and 127 MPa for the perpendicular and parallel bending orientations, respectively. The multi-wire slurry sawn (PV, slurry) wafers have a fracture strength in-between the two cases of DWS wafers, with a characteristic strength of approximately 140 MPa. It can be seen that the fracture strength of the as-cut wafers is generally lower than the etched or polished wafers. Weibull moduli calculated for these measurements are in the range of 4 to 12, with lower moduli for CMP wafers and higher moduli for PV wafers.

The fracture strength difference in the wafers can be explained by their surface morphology variation. Fig. 2 shows the surface topographical images for four different wafer surfaces. The CMP polished surface shows the greatest smoothness, with an areal surface roughness of less than 0.01 μm (Fig. 2a). It is clear that the CMP process has removed all rough edges and surface damage, which leads to the highest fracture strength. In contrast, the lapped and ground surface is much rougher, with an areal surface roughness of 0.32 μm, even after the damage-removal process (Fig. 2b). The rough surface and large surface height variation correlate to the low fracture strength in this case. The multi-wire slurry sawn surface has a similar feature as the ground surface but with a smaller pit size (Fig. 2c). The surface roughness is approximately 0.29 μm, and pit sizes are in the 5 to 10 μm range. The diamond wire sawn surface shows significantly different features from the other cases. The surface is very directional with many long parallel grooves mixed with a few pits (Fig. 2d). The surface roughness of DWS wafers is relatively low, at 0.17 μm.

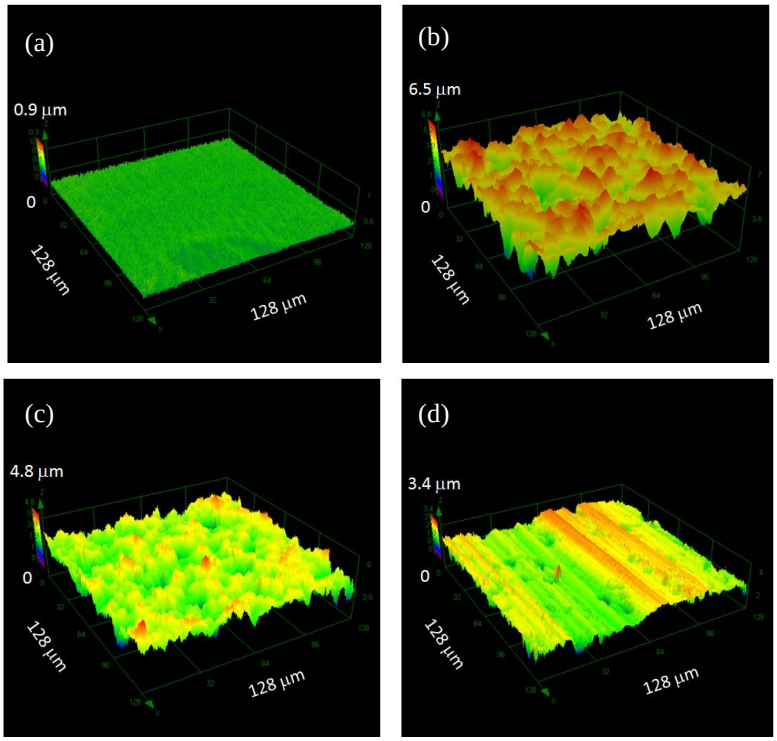

Fig. 2 Surface topographical maps measured by a 3D laser confocal microscopy. (a) CMP polished surface, (b) rough side of one-side polished wafer, (c) slurry sawn wafer, (d) diamond wire sawn wafer

In addition to the surface roughness difference, there are also surface and subsurface damage differences among these wafers. Fig. 3 shows the SEM images of the two different wire sawn surfaces (slurry vs. diamond wire sawing). Random pits are clearly observed on the slurry sawn surface due to the three-body material removal process (Fig. 3a). These pits are usually smooth and round due to the rolling grits and hydrodynamic contact present in slurry wire sawing. Also there are only a few small microcracks observed on the slurry sawn surface. On the contrary, the diamond wire sawn surface consists of many grooves and large pits (Fig. 3b). Long microcracks are often observed in the pitting area. The microcrack difference can be further seen on the bevel-polished surfaces. Only shallow subsurface microcracks (less than 0.8 μm) are observed in the slurry sawn wafers (Fig. 3c), but large subsurface microcracks (up to 4 μm in length) exist in the diamond wire sawn wafers (Fig. 3d). It is asserted that the long scratching grooves and the associated microcracks cause the fracture strength anisotropy observed in the diamond wire sawn wafers.

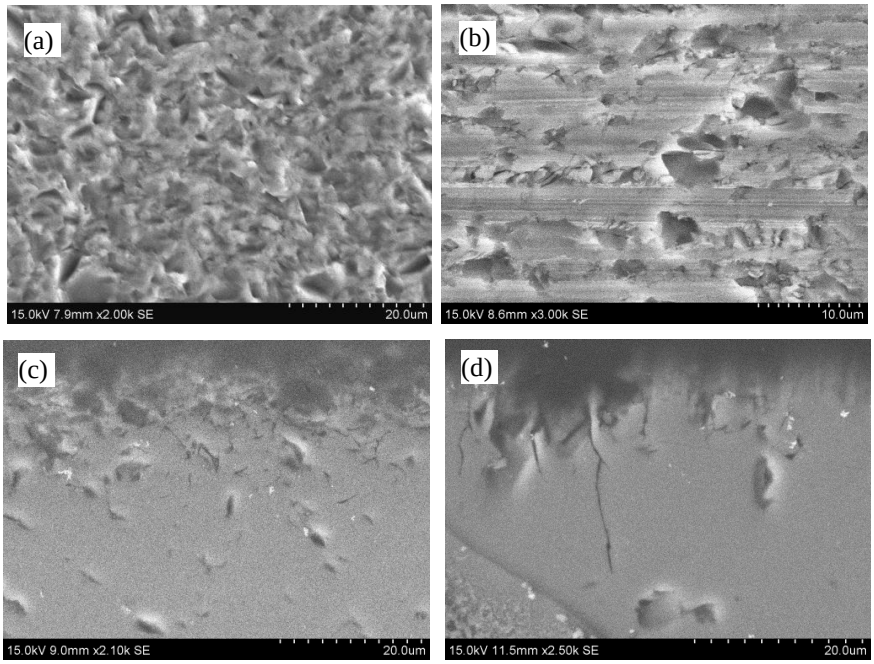

Fig. 3 SEM images of (a) slurry sawn surface and (b) diamond wire sawn surface, (c) and (d) are the corresponding subsurface damage after bevel polishing

A. Effect of Edge Defects

Edge defects are associated with process discontinuities at entry or exit, where chipping due to brittle fracture usually occurs. Fig. 4 shows a representative image of edge chipping on a silicon wafer after dicing. The dimension of chipping is dependent on the load. For the dicing process studied here, there will be an increase in chipping size with increase in the feed rate due to the increased contact force. Edge defects are observed on the smooth and rough surfaces of the IC wafers.

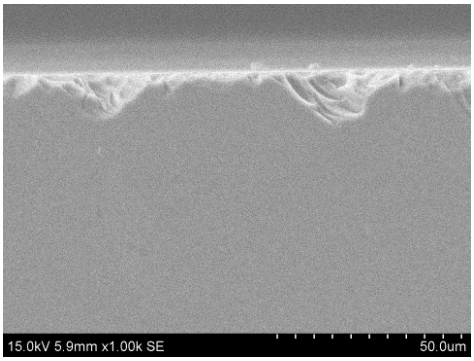

Fig. 4 A representative image of edge chips from wafer dicing

Fig. 5 shows the correlation of fracture strength with the dicing feed rate. It can be seen that there is a different trend for different surfaces. When bending with the smooth surface facing down (SSD), there is a gradually decreasing fracture strength with increasing feed rate. When bending with the rough surface facing down (RSD), however, the feed rate has almost no effect on the fracture strength. These results indicate that the effect of edge defects caused by dicing that was used to create the samples on the fracture strength depends on the surface defects. For a rough surface, the edge defect will be overwhelmed by the surface defects, which leads to less or no effect on the fracture strength. For a smooth surface, the edge defects become prominent due to their relative significance. In fact, the edge defects produced by the 12.7 mm/s feed rate are so significant that the fracture strength of the smooth surface (SSD) is close to that of RSD.

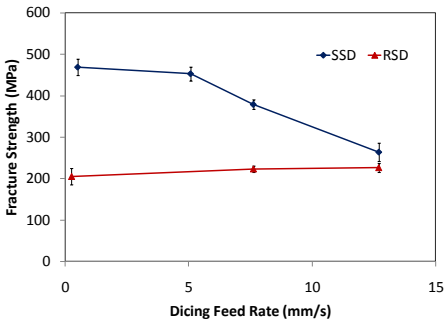

Fig. 5 Relationship of fracture strength with dicing feed rate for two different surface and bending conditions [3]

Fig. 6 shows a correlation of the physical defect dimension and the theoretically calculated defect size. The physical defects were measured as the largest chipping dimension on a surface. The theoretical defect size was calculated from the Griffith equation as, $K_{IC} = 1.12\sigma\sqrt{\pi a_c}$ with $K_{IC} = 0.95MPa\sqrt{m}$ [3, 13]. A good linearity with a coefficient greater than 0.995 is found between the measured and calculated defect sizes. Figs. 5 and 6 indicate the various roles of edge defects on the mechanical strength of silicon wafers. For a polished wafer, it is important to minimize edge defects so as to improve the mechanical integrity of silicon wafers.

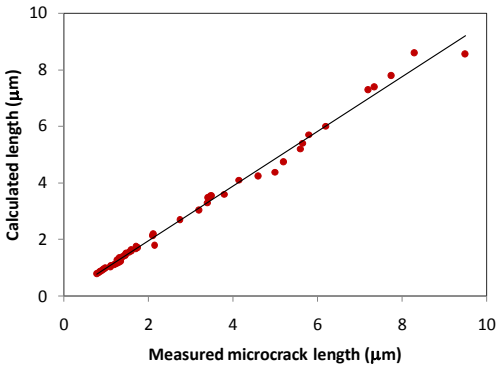

Fig. 6 A representative image of edge chips from wafer dicing

B. Cutting Mechanisms of Silicon

From the above results, it can be seen that the mechanical properties of silicon are critically dependent on the material removal process. Even though these processes vary greatly, they all have a common feature of utilizing contact between hard abrasive grits and silicon during the tribological interaction. This contact results in a micro-fracturing process where hard abrasive grits indent on brittle semiconductor materials on a microscopic scale. The load transferred to the semiconductor material during contact creates median and radial cracks. Upon unloading of the contact area the median cracks close up or interact with other cracks and the free surface leading to material removal. The material removal rate is basically a function of the external load and material properties, given by, for example, in a three-body removal process [14, 15]:

$$V_i = \alpha \frac{E^{5/4}}{K_{1c} H^2} P_i^{7/4} \tag{3}$$

where V_i is the volume of semiconductor material removed per indentation, P is the normal load per load-bearing particle, $\boldsymbol{E}$ and H are Young's modulus and hardness of the semiconductor material, α is a constant depending on particle shape.

The material removal process also leads to surface roughness that is dependent on the fracturing process. The average peak-to-valley roughness for the above case is related to the contact load as:

$$R_z = \alpha \frac{E^{1/2}}{H} P_i^{1/2} \tag{4}$$

For fixed abrasive machining (e.g. grinding or diamond wire sawing), the material removal rate will be greatly affected by the contact load and the distance travelled. For example, the material removal rate is proportional to the contact load and speed, as described by the Archard or Preston equation [2]:

$$V_i = kPv \tag{5}$$

where P is the normal load, v is the relative speed, k is a coefficient related to the surface contact condition. For each process, there will be a different material removal rate and surface smoothness. High speed or high pressure contact is crucial for a fast material removal in the two-body removal process. However, three-body removal and low contact force will improve the surface quality.

Lubricants used in the cutting/polishing process are also important in determining the material removal and surface finish characteristics. As a semiconductor process usually involves cutting grooves, lubricants not only actively remove swarf from the grooves, but also prevent adhesive contact between the cutting surface and the work piece. A direct or partial-contact is thought to occur in slurry sawing [16, 17]. The lubricants will also exert shear stress that can increase the material removal rate. It is also found that there will be additional suction force from the hydrodynamic contact in CMP [2].

Unfortunately, the micro-fracturing process will also create microcracks on the surface and subsurface. Fig. 7 shows a schematic of a cutting channel in a silicon wafer. Generally, there will be more microcracks at the bottom of the contact than the side contacts due to contact pressure difference. In fact, the contact load difference is beneficial for the cutting process since high contact load at the bottom can improve the material removal rate, while a low contact force on both sides can create a smooth surface. A representative SEM image of a dicing groove with a flat bottom is shown in Fig. 7b for comparison. Even though the microcracks are not clear at this magnification, corner chipping is clearly visible. Various types of microcracks such as median, lateral, "umbrella", "chevron", "branch" and "fork" have been reported [18, 19]. The above results clearly show the detrimental effect of microcracks on the mechanical strength of silicon wafers. As silicon wafer thickness decreases, the impact of surface defects will increase due to the increased surface-to-volume ratio. It is therefore important to have a damage-free cutting/polishing process for semiconductor manufacturing. Even though it is brittle, silicon can be cut in the ductile mode [4]. In ductile mode cutting, the silicon exhibits plastic flow-like behaviour instead of brittle fracture. Surface and subsurface microcracks can be effectively prevented in ductile mode cutting, which can therefore improve the fracture strength and mechanical integrity of silicon wafers.

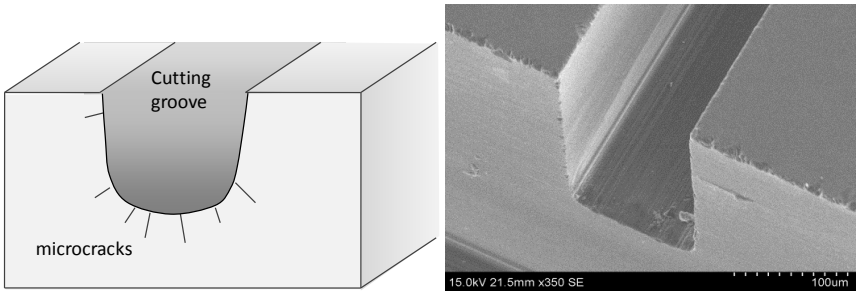

Fig. 7 A schematic of (a) a partial cut groove and (b) a SEM image of a dicing groove

IV. CONCLUSIONS

The fracture strength of silicon wafers is greatly affected by the surface created by tribological material removal in various semiconductor cutting and polishing processes. Tribological process induced defects can significantly reduce fracture strength, and include surface roughening, surface and subsurface microcracks, and edge chipping. Surface and subsurface microcracks can play a more significant role than edge chipping in determining the mechanical strength of silicon wafers. It is important to reduce the size of microcracks so as to improve the fracture strength of silicon wafers.

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