A Delta-Sigma Based Buck Converter - Design Methodology for Wireless Systems

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***Abstract*- Wireless systems customarily use LDO for excellent noise performance at the expense of poor power efficiency. Switching regulators using Pulse Width Modulation (PWM) controllers offer better efficiency but have greater magnitude spurs at multiples of the clock frequency. In this paper, a switching regulator that uses a delta sigma (ΔΣ) controller is considered as a substitute to provide both high power efficiency and improved spurious performance. Tradeoffs in selecting the ΔΣ parameters are investigated for several wireless standards such as WIFI, Bluetooth, GSM, W-CDMA, HSPA, LTE and WIMAX. Simulations in 0.5 μm CMOS technology, performed for key parameters such as spurious performance, efficiency and transient response show that the ΔΣ controller having 3rd order and over sampling ratio (OSR) of 32 can meet the stringent spectral conditions of a GSM system by a 10 dB margin. It also has 8% better power efficiency compared to the PWM controller. The performance of using this ΔΣ buck regulator for dynamically changing load applications is also analyzed. It is shown that for a 13% change in output voltage V_{OUT}, the ΔΣ buck regulator can still meet the spurious constraints of the GSM system.**

Keywords - Buck Converter; Delta Sigma Controller; PWM Controller; Wireless Applications; Wireless Standards; Noise Performance; Noise Shaping; Transient Performance; Envelope Tracking

I. INTRODUCTION

Wireless systems have strict spectral requirements which results in a low noise requirement for their power supplies. In addition, component sizes need to be small and efficiency should be high for extending battery life. LDOs typically regulate the output voltage by controlling the variably resistive pass transistor between the input V_{supply} and output voltage V_{OUT}. They offer exceptionally low ripple at the output and therefore can meet the spectral needs of wireless systems [1, 2]. However, their efficiency is low since they constantly dissipate power across the pass transistor that is biased in the linear region.

Most switching regulators used today typically have PWM as the control scheme for regulation [3]. These controllers switch every clock cycle to maintain the regulated output voltage [3]. The block diagram in Fig. 1 shows a buck converter using a PWM controller. The control loop consists of feedback resistors, an error amplifier with built in compensation (not shown in figure) and the PWM Controller [3]. The DR node, which is the controller output, causes transistors Q1 and Q2 to periodically switch at the clock frequency F_{clk}. As a result, the waveform at the SW node resembles a square wave with frequency F_{clk} [2]. By adjusting the duty cycle of the square waveform in the SW node, different output voltages can be achieved. The low pass filter formed by L1, C_{OUT} and its parasitic resistance (ESR) together help provide the averaged output.

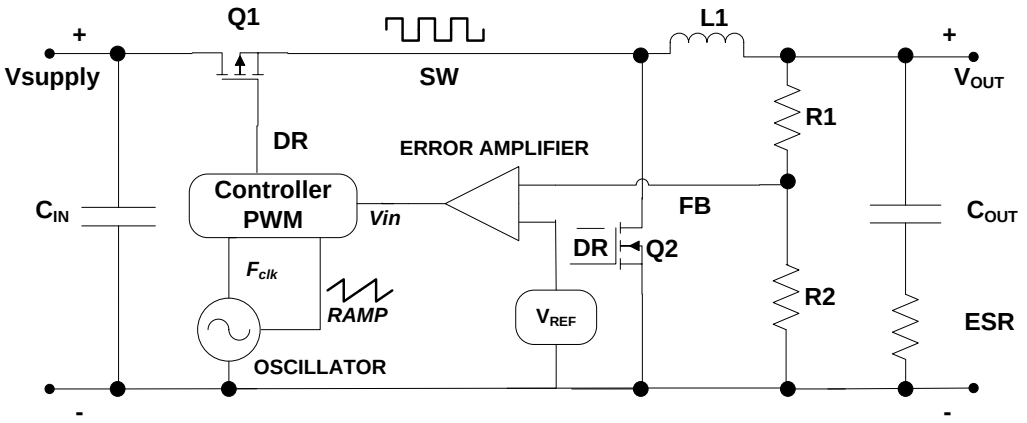
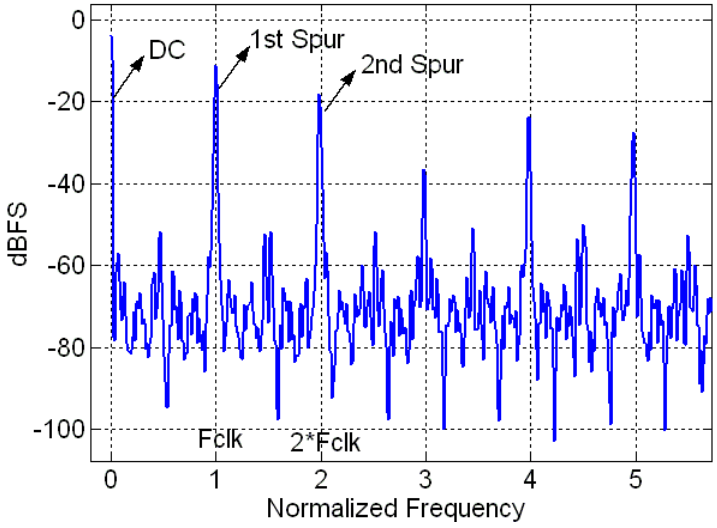


Fig. 1 Block diagram of a buck converter

Since the inductor and switches Q1 and Q2 have relatively low power loss compared to the variable resistor in the LDO, switching regulators have higher power efficiency at the expense of a more complex architecture and poor noise performance [2, 4]. The switching noise manifests itself in the form of ripple at the output in the time domain and as spurs at discrete multiples of the clock frequency (F_{clk}) in the frequency domain [2]. This noise then directly couples into the components that draw current from the regulator [2]. By selecting the filter 3 dB frequency to be much smaller than the clock frequency, an output voltage that has a very small ripple can be obtained [2-4].

Many alternative control techniques for EMI reduction such as non-linear control [5], anti-control for power converters [6], fuzzy control for output voltage ripple reduction [7] and addition of dithering to conventional PWM buck regulators [8] have all been explored. Another control technique that has gained attention in the recent years, uses the noise shaping characteristics of the ΔΣ modulator to reduce the clock spurs of the PWM [2, 3, 9, 10, 15] and thereby also helps reduce EMI [11-14]. It has been shown that the ΔΣ can replace the PWM controller in Fig. 1 and still retain stability and obtain better power efficiency than that of the traditional switching regulator [2, 3, 15]. ΔΣ modulators consist of integrators connected in a feedback loop so that the average output equals the average of the input signal [3]. The quantization noise gets shaped by this feedback; which causes most of its energy to be placed outside the signal band. This noise shaping property of the ΔΣ modulator causes randomization in the switching of the SW node of Fig. 1, so that transistors Q1 and Q2 may not switch every clock cycle [3]. The ΔΣ controller produces a variable sequence of pulses that is dependent on the output voltage, thereby distributing the switching energy away from the clock frequency F_{clk}. This reduces the magnitude of the spurs at F_{clk} [2]. Consequently, the average frequency at the SW node (F_{SW}) is dependent on the output voltage [2, 3].

The spurious performance of switching regulators needs to be superior to the specifications of the wireless systems they are powering [2]. The magnitude and location of these spurs define the type of filtering that is essential and therefore need to be carefully studied [2]. The spurs of the PWM and ΔΣ controller obtained from previous work [2, 3] are presented again in Fig. 2 for clarity. From the figure it is clearly seen that the ΔΣ controller has less magnitude spurs when compared to the PWM at F_{clk} but has spurs occurring at frequencies lower than F_{clk} [2].



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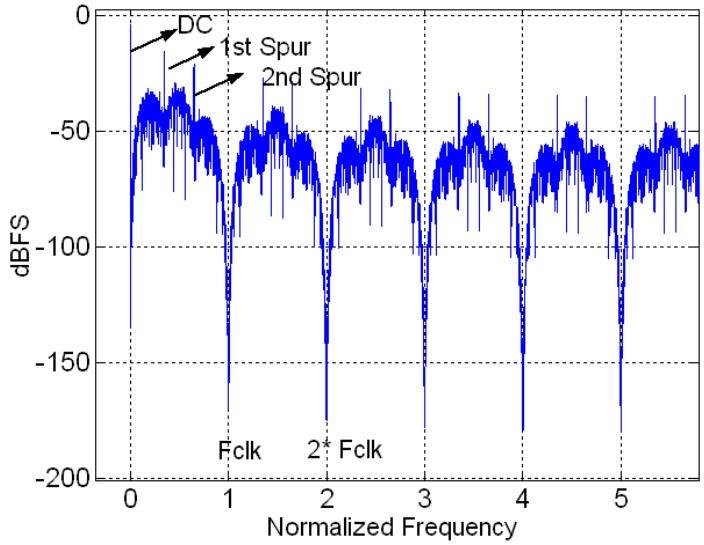


b)

Fig. 2 FFT of DR node of Fig. 1 for a) PWM and b) ΔΣ based buck converters showing 1st and 2nd spurs. F_{clk} =12.6 MHz. [2,3]

This paper examines how the ΔΣ buck regulator can be used to power various wireless systems. While previous work [2, 3] provided a design selection for GSM system based on ideal Matlab models, this work first extends to include other wireless

systems. It then provides a guideline on the transistor level design of the selected system and compares the spurious performance of this SPICE design against the wireless spectral requirement. In addition, it also looks in detail at the power efficiency, the line and load regulation and the transient performance of this implementation. Section II describes the spectral requirements for the different wireless standards and compares the spurious performance of existing PWM regulators against these prerequisites. It then illustrates how to make a design choice for a ΔΣ buck converter that can be used to power these wireless systems. This section also explores the impact of adding dither to the conventional PWM systems and compares these results with the GSM spectral requirements. Section III then describes the transistor level implementation of the selected ΔΣ buck regulator design. Section IV compares the power efficiency of both the PWM and ΔΣ modulators by examining the various losses commonly encountered in the systems. Section V then studies the impact of load change on the selected ΔΣ system. This section concludes by looking into the possibility of using the ΔΣ buck regulator for dynamically changing load applications for today's wireless systems.

II. WIRELESS SPECTRAL REQUIREMENT

A. Wireless Standards

GSM, WIFI, Bluetooth and W-CDMA are some of the well-established mobile telephony standards used extensively in modern wireless communication systems [2, 16]. Within the signal bandwidth referred to as in-band, the spur requirement for the system is determined by the signal to noise ratio (SNR) specification [2]. The spurs that occur in the out-of-band region are constrained by the spectral mask of the wireless standards. The signal bandwidth and the SNR requirements of these standards and some of the latest emerging wireless standards such as HSPA, LTE and WIMAX are listed in Table 1 [16-27].

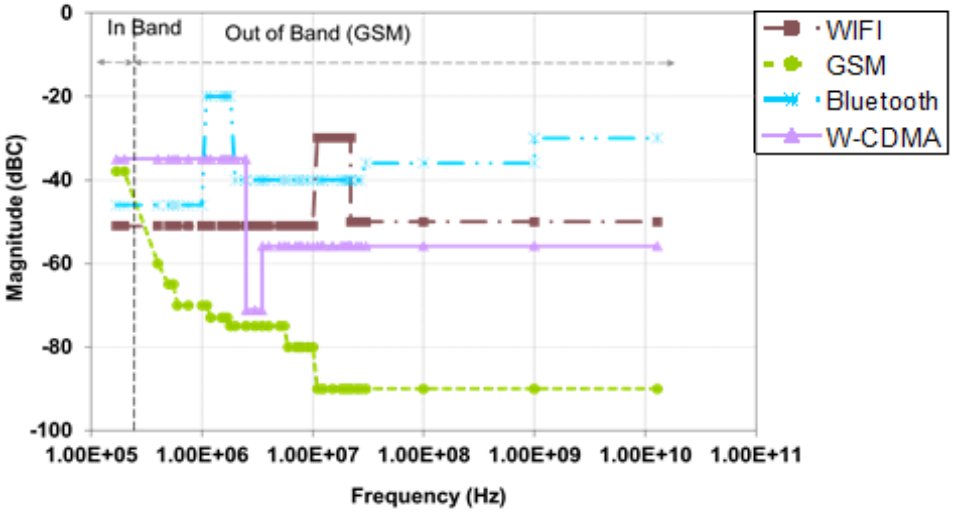
TABLE 1 WIRELESS STANDARDS AND THEIR IN-BAND SPECIFICATIONS

Wireless Standard	Bandwidth (MHz)	SNR (dB)
Bluetooth	1	20
W-CDMA	2.5	9
WIFI	11	25
GSM	0.17	12
HSPA	2.5	15
LTE	1000	10
WIMAX	1.8	18

In addition to the specified SNR values for these wireless standards, an extra 20 dB margin is added to ensure that the regulator spurs do not limit system performance [22]. Using an additional 6 dB as a designer's rule of thumb makes sure that all the spurs are below the necessary SNR specification [2]. Thus the in-band spurious performance requirement for the regulator is given by [2]

$$SNR_{Regulator}\,(dBC) \geq SNR_{Wireless} + 20 + 6 \quad (1)$$

A designer's rule of thumb of 8-10 dB margin is used for the spurs in the out-of-band region [2]. Taking these constraints directly from [16-27], Fig.3a and Fig.3b plot the spectral mask requirement of the wireless standards that should be met by the regulator used to power these systems.



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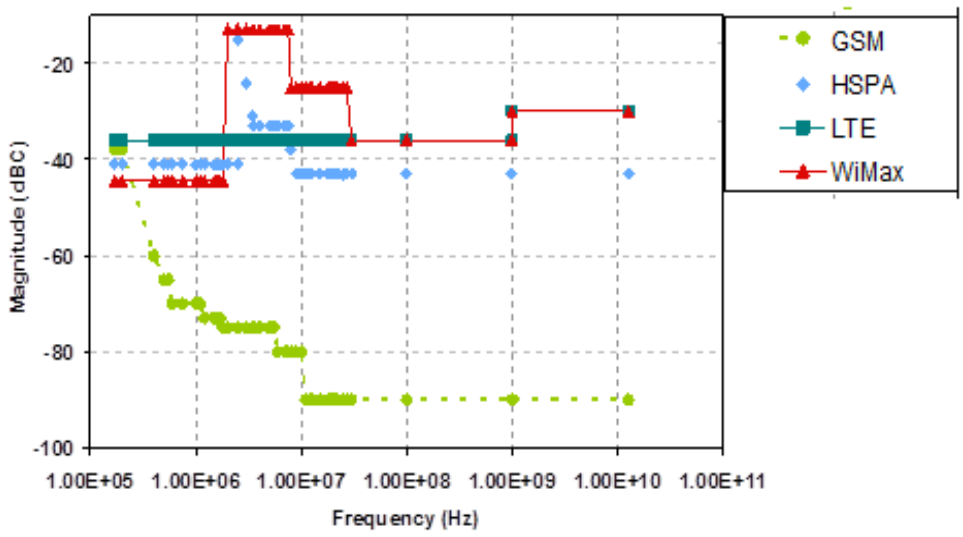


b)

Fig. 3 Spectral mask requirment a) Well established wireless standards such as GSM, WIFI W-CDMA and Bluetooth
b) Emerging technologies such as HSPA, LTE and WIMAX compared against GSM

From Table 1 and the plot it is seen that while the SNR of Bluetooth, WIFI, HSPA and WIMAX are higher than the GSM standard, the GSM still has the most stringent spur requirement in the high frequency out-of-band region compared to all standards. As a result, it is repeated in Fig. 3b as well. The buck regulators used for powering these wireless systems would require certain specific system setup conditions in order to meet these requirements. The next subsection describes these conditions in detail.

B. System Setup Conditions

Table 2 reviews the system requirements that are typically assumed for the buck regulator powering wireless applications. Most buck regulators in this application are powered by batteries whose input can vary from 2.7 V to 5.5 V and have a nominal value of 3.6 V [28-30]. Typically, the load current requirements of these buck regulators can range from 100 mA to a maximum of 2 A [28-30]. Hence the maximum load of 2 A was used for this study. One of the operating points for the buck regulators used in these applications is to have a V_{Supply} of 5 V stepping down to V_{OUT} of 3.3 V. This results in a duty cycle of 65%. Using the same duty cycle results in a V_{OUT} of 2.3 V for the 3.6 V V_{supply}. The average switching frequency (F_{sw}) of buck regulators used in this application ranges between 2-4 MHz [28-30]. The bandwidth of the buck regulator is determined by the maximum in-band frequency of the wireless standard it is powering. Since the signal bandwidth of the GSM system is 170 KHz, the bandwidth of the buck regulator was chosen to be 200 KHz. The inductor and capacitor values are chosen so that the ripple current is less than 30% of the maximum load current and the output voltage ripple is less than 1% of V_{OUT} for a given switching frequency of the regulator [4]. Their choice is also governed by their small form factor as wireless applications require small component sizes for easy integration. For this application, the 1 µH inductor and 10 µF capacitor were chosen to meet the requirements for the 2 MHz PWM switching regulator. This filter also results in a 3 dB frequency of 50 KHz. The on resistances, gate capacitances and the fall and rise time of the switches are selected to keep the power losses at a minimum. These parameters are process technology dependent. The values shown in Table 2 are based on Micrel Inc's 0.5 µm CMOS process technology [31].

TABLE 2 SYSTEM SETUP FOR THE BUCK REGULATOR [2]

Parameters	**Value**
Inductor L1	1 µH
Output Capacitor, C_{OUT}	10 µF
V_{Supply}	3.6 V
V_{OUT}	2.3 V
Iload	2 A
Switching Frequency (F_{SW})	2-4 MHz
Bandwidth	200 KHz
Switch Resistance (Q1,Q2)	25 mΩ
Gate Capacitance, Cg	5 nF
Clock Rise and Fall time	2.5 ns

C. *Spurious Performance of PWM Controller*

To determine whether the PWM buck regulators can meet the spectral mask requirements of the different wireless standards; their spurious performance is plotted in Fig. 4. The spectral masks of the well-established wireless standards that were shown in Fig. 3a are also repeated in this figure. These buck regulators were modeled using a duty cycle modulated pulse waveform in Matlab™ having different switching frequencies [2, 3]. The spur magnitudes for these regulators are obtained by filtering the spurs using the L1 and C_{OUT} filter described in Table 2.

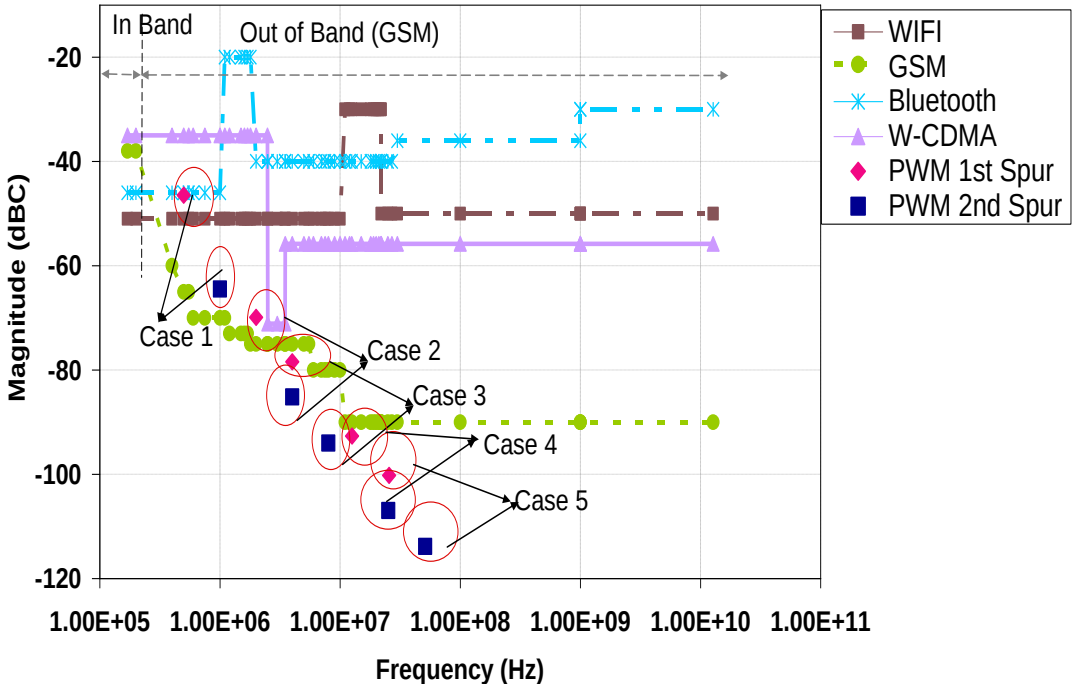


Fig. 4 Spectral mask requirement of the wireless standards such as GSM, WIFI W-CDMA and Bluetooth along with the filtered spur magnitude of the PWM modulator. Case 1: Fclk=0.5 MHz, Case 2: Fclk=2 MHz, Case 3: Fclk=4 MHz , Case 4: Fclk=12.6 MHz and Case 5: Fclk=25.6 MHz

Case 1 in Fig. 4 shows that the spurs of the PWM having a switching frequency of 500 KHz, barely meets the spur requirement of Bluetooth and W-CDMA standards while it does not meet that of WIFI and GSM. Case 2 shows the spurs corresponding to switching frequency of 2 MHz meet the spectral requirement of both Bluetooth and WIFI but fail to meet that of W-CDMA and GSM. Case 3 and Case 4, which show the PWM buck regulators having a switching frequency of 4 MHz and 12.6 MHz respectively, meet the Bluetooth, WIFI and W-CDMA requirements but not that of GSM. Finally, Case 5, which has a switching frequency of 25.6 MHz, meets all the shown wireless standards. Even though the PWM controller switching at high clock frequencies meets the spectral requirements, it has poor power efficiency due to larger switching losses and hence is not a practical design solution for these standards [6].

D. *ΔΣ Design Selection*

An alternate architecture using a ΔΣ controller can be optimized to meet the requirements of the wireless systems [2]. The performance of the ΔΣ controller is dependent on its input voltage (V_{in}) relative to full scale voltage ($V_{Fullscale}$), the OSR and the order [2, 3]. The ΔΣ toolbox in Matlab™ was used to create the controller models [2, 3, 32]. The input and the logic levels in the Matlab toolbox are scaled to range from 0 to 1, with 0 corresponding to the logic low and 1 corresponding to $V_{Fullscale}$ value. In this application, the $V_{Fullscale}$ was chosen to equal V_{supply} and V_{in} was selected to be V_{OUT}. The system settings and the output filter for the ΔΣ buck controller are presumed to be identical to that of the PWM system described in Table 2. The effect of the variation of V_{in} and OSR on the spur magnitude and location has been studied in detail in previous work [2, 3]. For the V_{supply} and V_{OUT} voltages described in Table 2, the corresponding $V_{in}/V_{Fullscale}$ ratio is 0.65 in the ΔΣ modulator. Using this setup and results from previous work [2], the spur magnitudes and frequencies of ΔΣ controller for different OSR and orders are plotted in Fig. 5. All the spurs of the ΔΣ modulator occur in the out-of-band region [2]. Since the GSM standard has the most stringent spectral mask requirement in this region, it is also plotted in Fig. 5.

The same 8-10 dB margin that was detailed in Subsection A in this section is used for comparison of the filtered spurs against the GSM spectral mask. Case 6 in Fig. 5 corresponds to the 2nd order system with OSR of 128 that can meet the GSM spectral requirement with 10 dB of margin. Case 7 which represents the 3rd order ΔΣ system with OSR 32, meets this constraint for both the first and second spurs by 12 dB margin. Since the higher order 4th and 5th order modulators show very little improvement in spur magnitude and location [2] but have increased design complexity, the 3rd order was chosen as an appropriate design choice for this application.

Just like the ΔΣ modulator shapes the noise and moves the spurs to higher frequencies, alternate techniques such as dithering have been used to lessen the spur magnitude of the PWM based buck converters as described in Section I. The next section studies the impact of adding dither to regular PWM buck regulators and examines their performance from the wireless system application point of view.

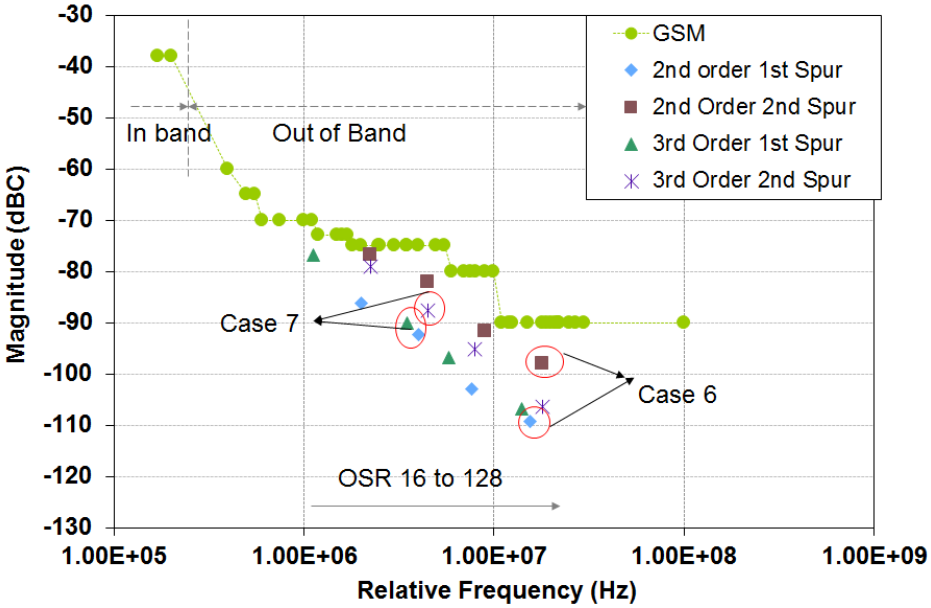
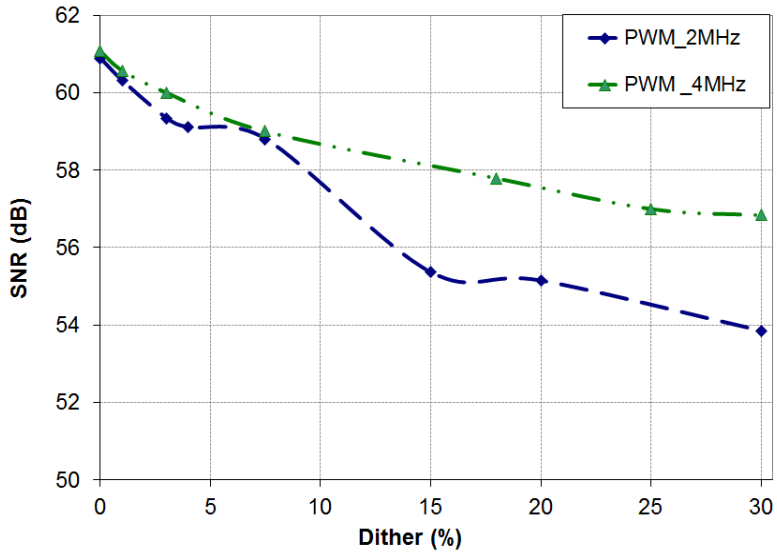


Fig. 5 Spectral mask for GSM wireless system along with the spur magnitude after filtering a 2nd and 3rd order ΔΣ modulator for Vin/$V_{Fullscale}$=0.65. The four points in each graph correspond to OSR of 16, 32, 64 and 128. Case 6: 2nd Order with OSR=128 Case 7: 3rd Order with OSR=32. [2]

E. Effect of Dither on PWM Systems

The addition of dither to regular PWM systems is predominantly used to decrease EMI by reducing the spur magnitude at the expense of increasing the noise floor [8, 33]. This section explores how the reduced spur magnitude of conventional PWM buck regulators by dither addition compares with the GSM spectral requirement. Pseudo random dither was introduced at the ramp node (shown in Fig. 1) for both the 2 MHz and 4 MHz PWM buck converters. Since the ramp is acquired from the oscillator as seen in Fig. 1, the addition of dither causes F_{clk} to proportionally change. For example, if a 10% dither is added to the buck converter, it causes the F_{clk} to also change by +/-10% of its fundamental frequency.

Fig. 6 studies the SNR reduction and the impact on spur magnitude of the 2 MHz and 4 MHz buck regulators due to addition of dither. These converters originally did not meet the GSM system's spectral constraint as inferred from Fig. 4. The effect of dither on the SNR is plotted in Fig. 6a. As the amount of added dither increases, the V_{OUT} ripple becomes larger thereby raising the noise floor which causes the SNR to decrease.



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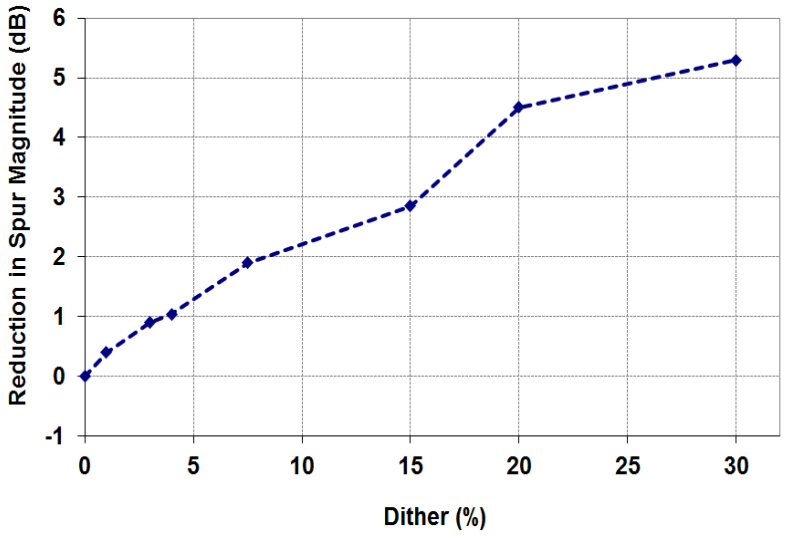
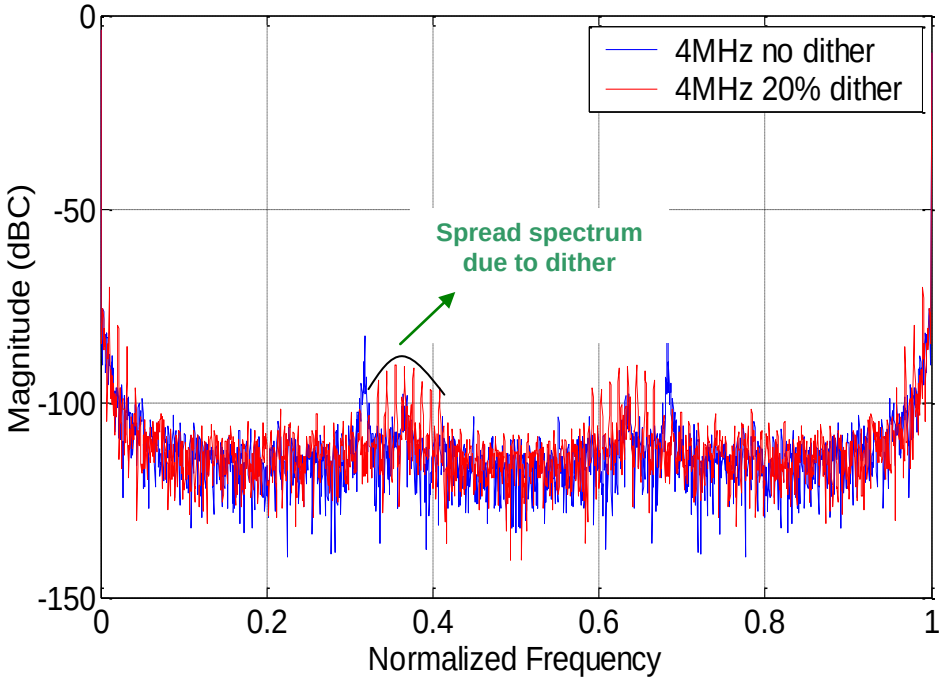


b)

Fig. 6 Dither characterization for PWM buck converters. a) Reduction of in-band SNR vs % Dither. b) Reduction of Spur magnitude with % Dither.

V_{OUT} ripple also decreases as the switching frequency increases. As a result, the SNR of the 4MHz buck regulator is larger than the 2 MHz PWM buck regulator and does not change by a significant amount for the entire range of added dither. Fig. 6b plots the effect of dither on the spur magnitude. As more dither is added, the energy of the spur gets spread over larger frequency bins thereby reducing the spur magnitude. As a result, this curve, which plots the reduction in spur magnitude with dither, is linear. This concept can be understood from Fig. 7a which compares the FFT spectrum of the regular and the 20% dithered 4 MHz buck regulators. The spectrum spreading and subsequent spur magnitude reduction due to dither is clearly seen from this plot. The 20% dither value was selected as it provides sufficient spur magnitude reduction along with less than 6 dB change in its SNR.

Fig. 7b compares the spur magnitudes of the 20% dithered 2 MHz and 4 MHz PWM buck regulators against the GSM spectral mask. From the figure it is observed that while the 2 MHz PWM barely meets the GSM specification with 3 dB margin, the dithered 4 MHz PWM regulator can meet the requirement with 10 dB margin.



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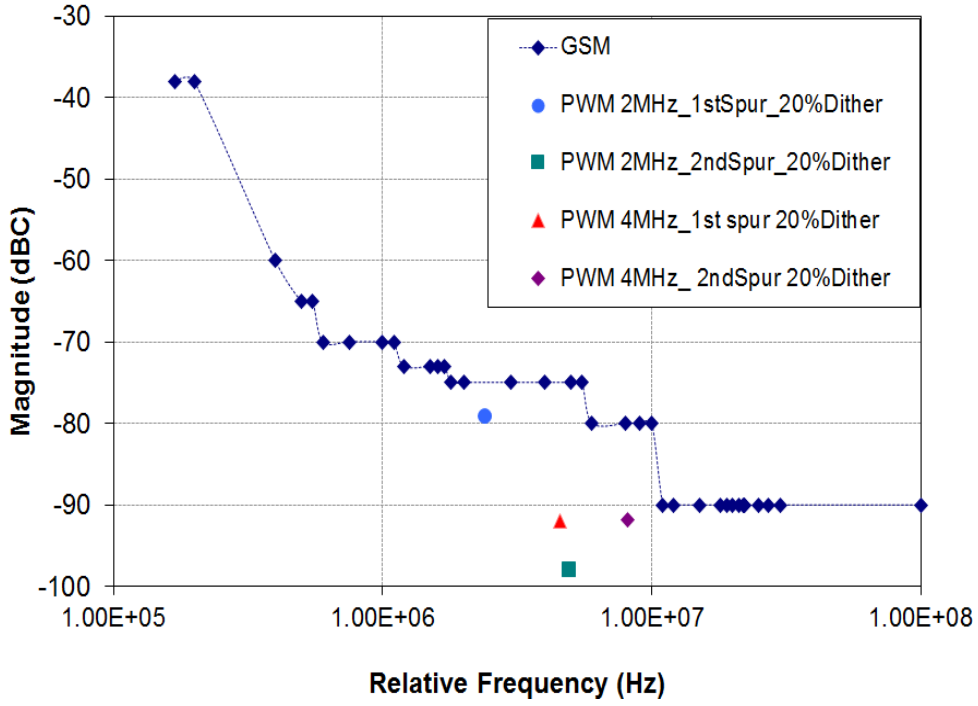

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Fig. 7 Dither characterization for PWM buck converters. a) FFT spectrum comparison between regular and 20% dithered 4MHz PWM buck regulators. b) Spurious performance of the dithered PWM buck regualtors against the GSM spectral mask.

Fig. 8 compares the FFT noise spectrum of the selected 3rd order ΔΣ system against the regular and the dithered 4 MHz PWM buck regulators. Since this work compares the results of converters that are switching at different frequencies, a normalized frequency axis is used in the figure. From the figure it is perceived that the ΔΣ system shows significant reduction of 10 dB in spur magnitude when compared to the regular 4 MHz PWM buck regulator. Its spur magnitude is about the same as the 20% dithered PWM buck regulator.

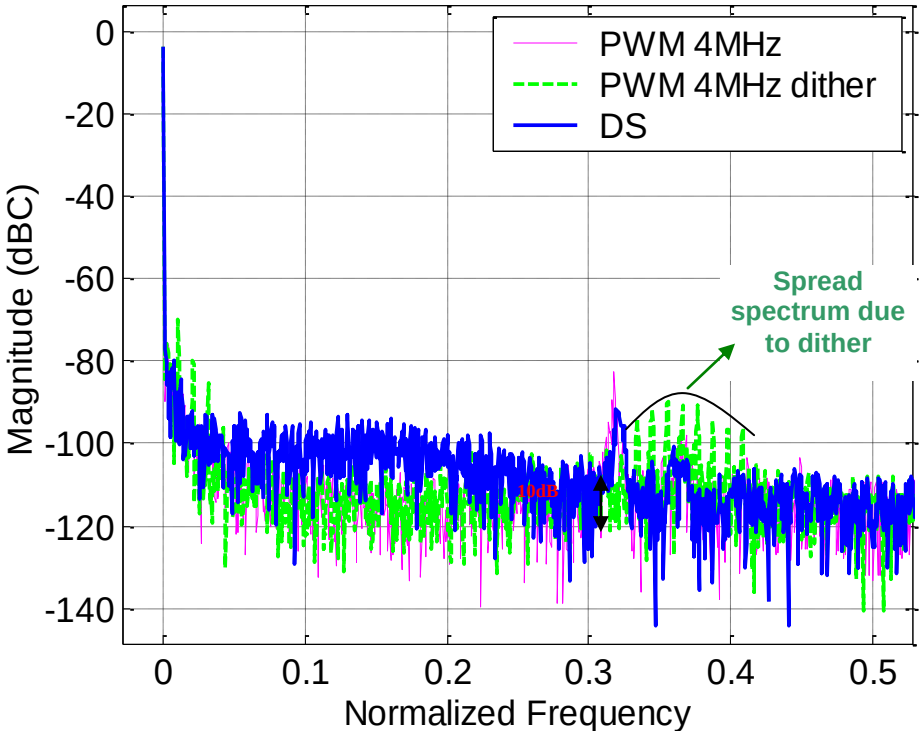


Fig. 8 FFT spectrum comparison of the 3rd order, OSR =32 ΔΣ controller against the regular and 20% dithered 4 MHz PWM buck regulators

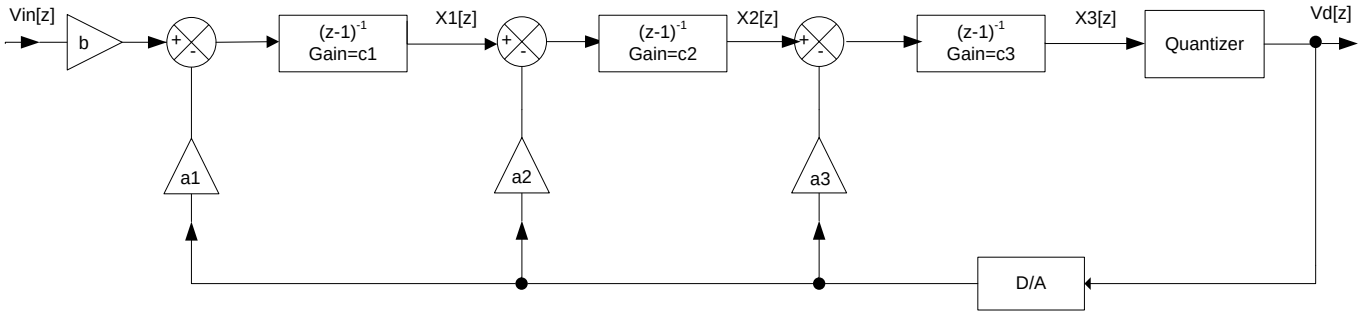
Therefore, while the addition of dither can make the high frequency PWM buck regulator meet the wireless standard's spectral mask constraints, its power efficiency can get compromised which is discussed in Section IV.

III. DESIGN OF ΔΣ BUCK REGULATOR

The design process for the implementation of the selected 3rd order ΔΣ system with OSR 32 is described in the ensuing section.

A. *Theory*

One of the key requirements for the ΔΣ controller used in the buck converter is to have a sufficiently large degree of linearity and accuracy over the full input range [32]. To accommodate this, the discrete time ΔΣ architecture using switched capacitor integrators was selected. Fig. 9a presents the block diagram of the 3rd order ΔΣ modulator using the cascade of integrators in feedback form (CIFB) and Fig. 9b shows its circuit level implementation. This architecture was chosen for its simplicity, low harmonic distortion at the output, and ease of dynamic range scaling [32]. This system has an all pole signal transfer function (STF) given by (2) which resembles a low pass filter in the signal path. The quantization noise transfer function (NTF) given by (3) resembles a high pass filter.



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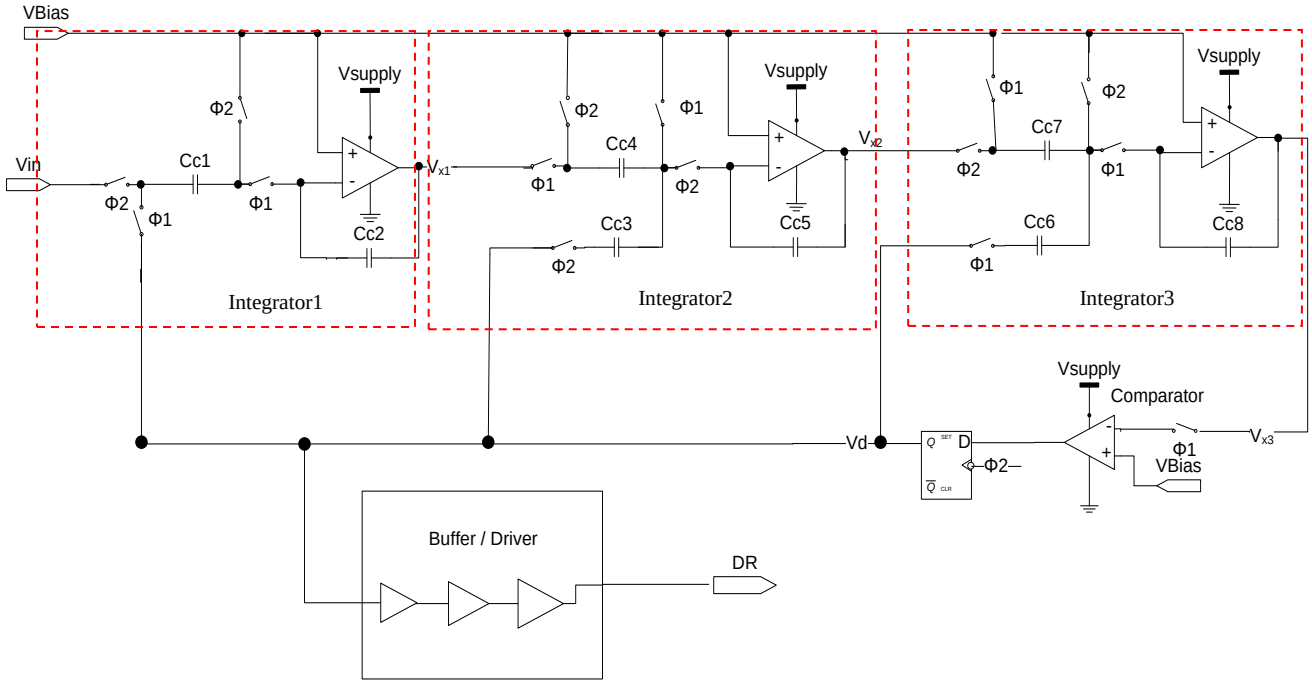


b)

Fig. 9 3rd order ΔΣ modulator a) Block diagram of CIFB configuration b) Switched capacitor implementation. VBias=Vsupply/2.

$$STF = \frac{b}{\left(\frac{(z-1)^3}{(c1*c2*c3)} + \frac{a3}{(c1*c2)}*(z-1)^2 + \frac{a2}{c1}*(z-1) + a1\right)} \quad (2)$$

$$NTF = \frac{\frac{(z-1)^3}{c1*c2*c3}}{\left(\frac{(z-1)}{(c1*c2*c3)}\right)^3 + \frac{a3}{(c1*c2)}*(z-1)^2 + \frac{a2}{c1}*(z-1) + a1)} \quad (3)$$

Where a1, a2 and a3 are the feedback gains of the integrators, c1, c2 and c3 represent the gains of the integrators and b is the factor by which the input is amplified.

Table 3 shows the optimal gain coefficients and the respective scaled gains for the switched capacitor integrators shown in Fig. 9b. Since the feedback gain and the input gain of the first integrator are the same, a single Cc1 capacitor is used [32, 34]. The 2nd and 3rd integrators follow the implementation as shown in Fig. 9b.

Fig. 9b also shows the phases of F_{clk} (Φ1 and Φ2) that are used to clock the integrators. For this design, the OSR of 32 and bandwidth of 200 kHz results in the F_{clk} given by

$$F_{clk}=2*OSR*bandwidth = 12.6 \text{ MHz} \quad (4)$$

TABLE 3 switch capacitor implementation for 3rd order δσ modulator

	Feed back gain	**Scaled gain for switch capacitor implementation**	**Integrator gain**	**Scaled gain for switch capacitor implementation**	**Gain at the input**
1st Integrator	a1=0.139	Cc1/Cc2=0.077	c1=0.3173	Cc1/Cc2=0.077	b=0.139
2nd Integrator	a2=0.2554	Cc4/Cc5=0.44	c2=0.2391	Cc3/Cc5=0.33	0
3rd Integrator	a3=0.1513	Cc7/Cc8=0.26	c3=6.1145	Cc6/Cc8=0.25	0

Since the SNR required by the buck converter is 38 dB for the GSM standard, a single ended implementation is sufficient for the operational amplifier used in the integrators. The non-idealities of this amplifier such as finite gain, offset and unity gain bandwidth affect the performance of the ΔΣ modulator [32, 35]. This performance is quantified by the in-band SNR, the spur magnitudes and frequencies and the signal to noise distortion ratio (SNDR). Simulations were performed on a SPICE macro model of the ΔΣ modulator, based on Fig. 9b, to determine the actual amplifier design specifications.

B. MacroModel Simulation Results

Simulations of finite amplifier gain showed the in-band SNR degradation as plotted in Fig. 10a. For gains larger than 55 dB, the SNR remained constant but decreased proportionately for lower gains. The change in the SNDR was less than 0.5 dB for amplifier gains greater than 50 dB. The spur magnitude and frequencies did not change with the gain. Based on these results, a minimum amplifier gain of 55 dB was chosen.

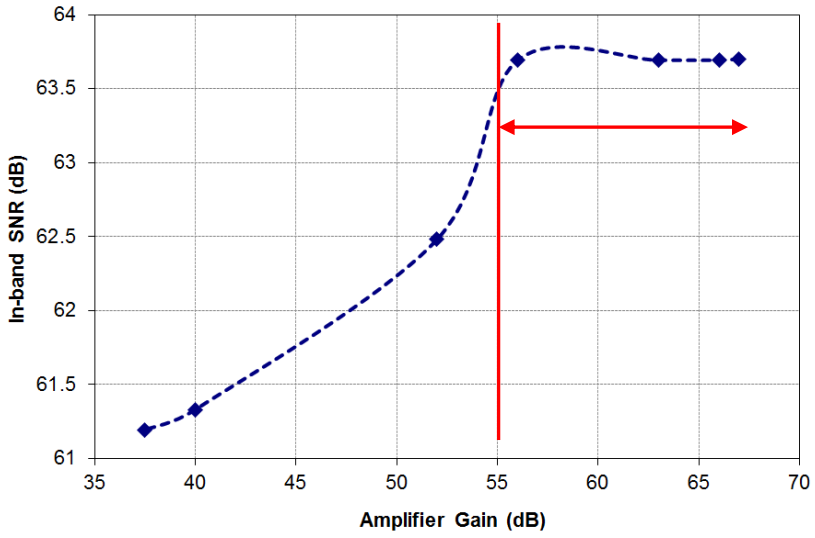
A Monte Carlo analysis was performed on the SPICE macro model to determine the impact of the input offset of the amplifier. These offsets were varied for all three amplifiers as this represents the worst case scenario. The typical 1 sigma offsets in 0.5 μm CMOS technology varies between -10 mV to 10 mV [31]. Simulation results for the 3 sigma offset showed very little variation in SNR. Fig. 10b plots the SNR degradation for a wider range of offset variation of the amplifiers. For this design from the simulations results, an offset variation of +/-10 mV was therefore chosen. The SNDR changed by less than 0.3 dB and the spurs did not change significantly for the above offset range.

The effect of unity gain bandwidth of the amplifier showed a similar trend as that of the finite gain. The SNR reduced by more than 6 dB for bandwidths less than 100 MHz as seen in Fig. 10c. For bandwidths higher than 200 MHz, the SNR remained constant. The SNDR reduced by 1 dB for lower bandwidths while the spur magnitudes and frequencies remained relatively constant.

Based on Fig. 10, the design specifications of the operational amplifiers that were utilized in the ΔΣ modulator are summarized in Table 4.

TABLE 4 OPERATIONAL AMPLIFIER SPECIFICATIONS

Amplifier Characteristics	**Design Specification**
Minimum Gain	50-60 (dB)
Maximum Offset at the input tolerated	+/-10 mV
Minimum Unity gain bandwidth	190-200 MHz



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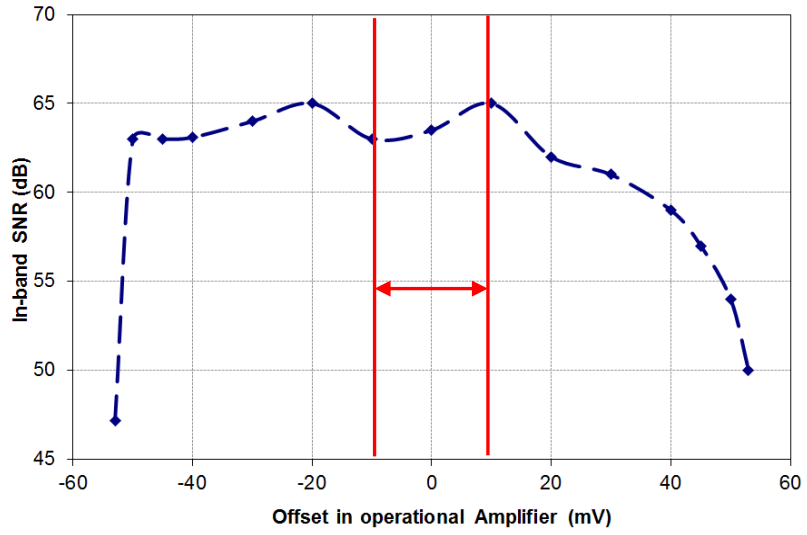

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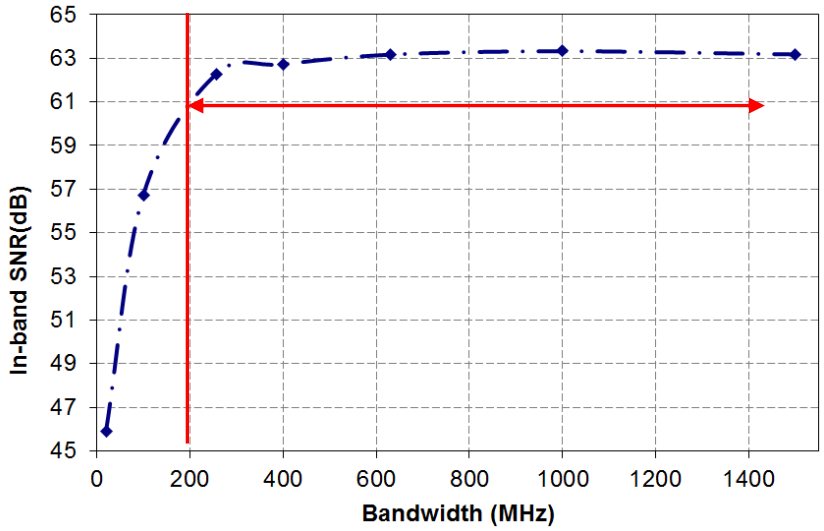


c)

Fig. 10 Effects of operational amplifier parameters such as a) Amplifier Gain b) Offset and c) Bandwidth on the in-band SNR

C. *Transistor Level Design*

Using the specifications from Table 4, a single ended folded cascade operational amplifier was chosen as the design architecture [34, 36, 37]. The minimum capacitance used for the switched capacitors was 1 pF to ensure that it is much larger than the typical parasitic and stray capacitances which typically range from 50-75 fF for 0.5 µm process technology. A tail current of 5.5 mA and a folded cascode load current of 2 mA ensure that the amplifier used in the first stage integrator can achieve 203 MHz unity gain bandwidth and 65° phase margin with a 15 pF load capacitor. The amplifiers used in the two subsequent integrators of the ΔΣ modulator can work at reduced currents as their gains and load capacitors are much smaller [32]. Therefore, for these two stages a tail current of 900 uA and the folded cascode load current of 700 uA can achieve 190 MHz and 60° phase margin with a load capacitor of 5 pF. The 1 bit quantizer architecture is a latched high speed comparator as shown in Fig. 9b. Its design is described in [30]. The output of the latched one bit quantizer is sampled into the integrators using the 1 bit DAC which is implemented as switches in Fig. 9b [30]. The total power consumed by this ΔΣ modulator for a $V_{in}/V_{Fullscale}$ of 0.65 is 50 mW which is much smaller compared to the switching and inductor losses that are encountered by buck regulators. These losses will be discussed in Section IV.

The buck converter designed using the above ΔΣ modulator has a SNR of 60 dB for a bandwidth of 200 KHz and a SNDR of 48 dB measured over a bandwidth of 6.3 MHz. Fig. 11 compares the spurs of this ΔΣ buck converter against the GSM spectral mask. From the figure it is seen that the designed ΔΣ buck regulator shows identical results with that of the ideal Matlab model described in [2] and therefore meets the GSM spur requirement with sufficient 10 dB margin.

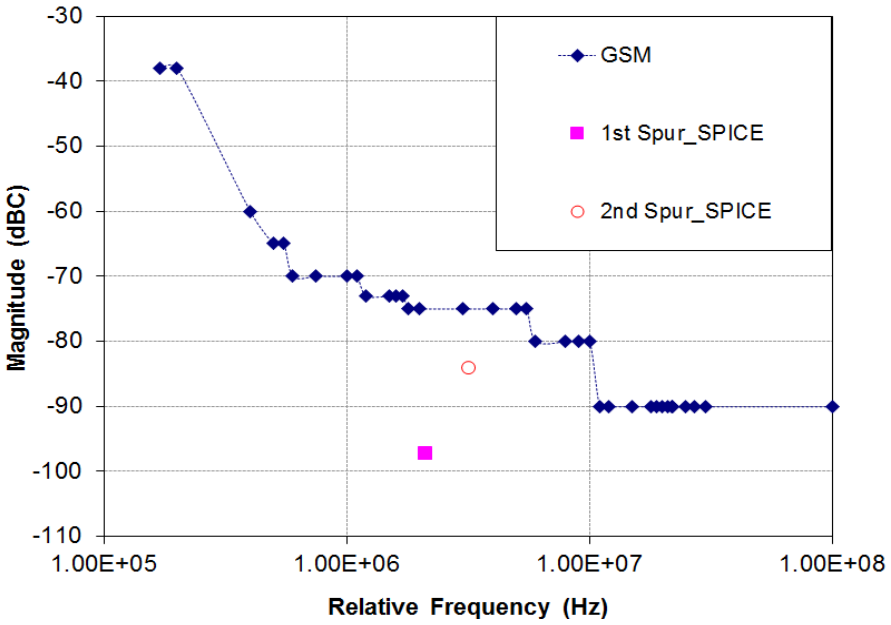


Fig. 11 Comparison of SPICE design for $V_{in}/V_{Fullscale}$ of 0.65 plotted against the GSM spectral mask. The F_{clk} of ΔΣ converter is 12.6 MHz.

IV. POWER EFFICIENCY

Power efficiency is one of the most critical specifications for switching regulators. It is measured by the ratio of the output power (P_{out}) to the input power (P_{supply}) [4]. The relationship between P_{supply} and P_{out} is given by Equations (5) and (6).

$$P_{supply} = P_{out} + P_{loss} \tag{5}$$

with

$$P_{loss} = P_{transient} + P_{Conduction} + P_{Cg} + P_{Deadtime} + P_{Moscap} + P_{static} + P_{Ind} \tag{6}$$

The loss terms can be split into two categories. They are: a) losses that occur at the SW node and b) the losses that occur in the inductor. In Section I, it was mentioned that the SW node resembles a pulse waveform that either switches periodically as in the PWM or as a stream of pulses as in the ΔΣ modulator. During the on time (T_{ON}) and off time (T_{OFF}) of the SW node, the loss terms that dominate are $P_{Conduction}$ which is the conduction loss due to the fixed on resistance of the switches Q1 and Q2; $P_{transient}$ which is the power loss from the set rise and fall times of the SW node; P_{Cg} which is the power lost in charging and discharging of the gate capacitance (Cg) of Q1 and Q2 during switching [3] and $P_{Deadtime}$ which is the loss that occurs due to the finite dead time when the body diode of the free-wheeling FET Q2 is turned on. P_{Moscap} is the loss that arises due to parasitic capacitance at the SW node. A 100 pF parasitic capacitance was assumed connected to the SW node to determine this loss term. These losses that occur in the SW node can be categorized as switching loss P_{sw}.

The losses in the inductor can be split into P_{static} which occurs due to the load current and the parasitic resistance (DCR) present in the inductor [3]; and P_{Ind} refers to the eddy current and skin effect losses that are again impacted by load currents and high switching frequency in the buck converter. In addition, most inductors have magnetic core losses which become significant at high frequency. The inductors that are commonly used in wireless applications such as those in [28-30] ensure that the magnetic core losses are minimal. One such typical inductor TDKRLF7030-1R0N6R4 that was used in [28] is considered for the design of the buck converters in this application. Its inductor loss P_{Ind} was modeled by a resistor R model placed in parallel with the inductor. This value is obtained from the datasheet and SPICE library of the inductor [38, 39]. The R model remained constant for switching frequencies ranging between 2 MHz and 12.6 MHz. This was verified with the power loss tool offered by TDK in [40]. As a result, the P_{Ind} loss remains constant for these frequencies. To calculate the core loss of the inductor the power tool requires the inductor's peak to peak ripple current and the load current I_{load} as inputs in addition to the switching frequency. Using the values of peak to peak ripple current of 0.5 A for 2 MHz, 0.4 A for 4 MHz and 0.2 A for 12.6 MHz, the core losses were found to be zero for these frequencies of interest as reported by the tool.

Table 5 compares the losses for the PWM systems and the 3rd order ΔΣ buck converter with OSR 32 both driving a load current of 2 A. The table also shows the equations associated with the loss terms. These equations clearly show the dependence of these loss terms on the switching frequency (F_{sw}). The 4 MHz buck regulator with dither is also included in the table. Since the dithered buck regulator's average switching frequency is identical to the regular 4 MHz buck regulator, the losses and consequently the efficiency of the two systems are equal. As mentioned in Section I, the F_{clk} and F_{sw} are the same for the PWM systems and the average F_{sw} for the ΔΣ is V_{in} dependent [2, 3, 32]. For the 65% duty cycle of the PWM and load current of 2 A, the equivalent $V_{in}/V_{Fullscale}$ ratio of the ΔΣ modulator causes its average F_{sw} to be 3.5 MHz with F_{clk} at 12.6 MHz. Since the PWM and the ΔΣ based buck converters differ only in the MOSFET gate drive waveform (DR node in Fig. 1) the DCR and the AC losses in the inductor are the same [3]. The other power losses, listed in Table 5 which are dependent on F_{sw}, contribute to the efficiency difference between the two systems.

TABLE 5 POWER LOSS AND EFFICIENCY CALCULATION FOR THE BUCK CONVERTERS

Loss Terms	Loss calculation	Losses (mW)					Notes
		PWM				ΔΣ	
		F_{clk}=2MHz F_{sw}=2MHz	F_{clk}=12.6MHz F_{sw}= 12.6MHz	F_{clk}=4MHz F_{sw}= 4MHz		F_{clk}=12.6MHz F_{sw}=3.5MHz	
				Regular	20% Dither		
$P_{Conduction}$	$((I_{load})^2*Rdson*T_{on}*F_{sw})+ (I_{load})^{2*}*Rdson*T_{off}*F_{sw})$	346	346	346	346	329	
$P_{transient}$	$(V_{Supply}*I_{Load}*(T_{Rise}+T_{Fall})*F_{sw})/2$	38	240	76	76	60.5	
$P_{DeadTime}$	$I_{Load}*V_{\ body\ diode}*(2*T_{Deadtime})*F_{sw}$	24	151	48	48	42	Assuming 5ns dead time
P_{Cg}	$2*Q_g*F_{sw}*V_{Supply}$	43.2	272	86.4	86.4	75.6	Using Qg=3pC, for both Q1 and Q2.
P_{Moscap}	$2*100pF*Fsw*(V_{Supply})^2$	5.18	32.7	10.4	10.4	9.07	
Inductor DCR Loss (P_{static})	$(I_{Load})^2$ * DCR	40	40	40	40	40	
Inductor AC Loss (P_{Ind})	$(V_{Supply}-V_{Out})^2/R_{model}$	0.815	0.815	0.815	0.815	0.815	
P_{Loss}	$P_{static} + P_{Ind} + P_{Conduction} + P_{Cg} + P_{Moscap} + P_{transient} + P_{Deadtime}$	497.195	1082.5	607.6	607.6	556.985	
P_{out}	$I_{Loas}*V_{out}$	4720					
Efficiency (%)		90.47	81.34	88.6	88.6	89.5	

From Table 5, it is clearly seen that higher frequencies contribute to larger switching losses which causes the efficiency to decrease. While the 2 MHz PWM buck regulator shows the best power efficiency compared to all the other systems, it fails to meet the spur requirements of the GSM system as shown in Section II. Higher frequency PWM regulators can meet the spurious conditions with dither but they show poor efficiency. The ΔΣ buck regulator on the other hand can meet the spectral mask constraints and also shows an increased efficiency of 0.9% and 8% when compared to the 4 MHz and the 12.6 MHz PWM converters at 2 A respectively.

To study the effect of different load currents on the efficiency, the SPICE implemented design of the ΔΣ, regular and dithered 4 MHz PWM buck converters were simulated for different $I_{load.}$ These PWM buck converters were chosen as they show similar spurious performance as the ΔΣ converter. Fig. 12 plots the power efficiency as a function of varying load current for these regulators. From the figure, it is seen that the efficiency of the implemented design is identical to the theoretical value shown in Table 5. The static losses in the inductor dominate for higher load currents which causes the efficiency to decrease. At lower load currents, the switching losses P_{sw} dominate and cause the low efficiency. The dithered and the regular PWM buck regulators show very little difference as expected from the theoretical analysis in Table 5. The ΔΣ buck regulator on the other hand shows better efficiency over all load currents compared to the dithered and the regular 4 MHz PWM buck

regulators. Therefore it is a better choice for powering GSM systems compared to the PWM buck regulators as both spurious performance and power efficiency need to be considered.

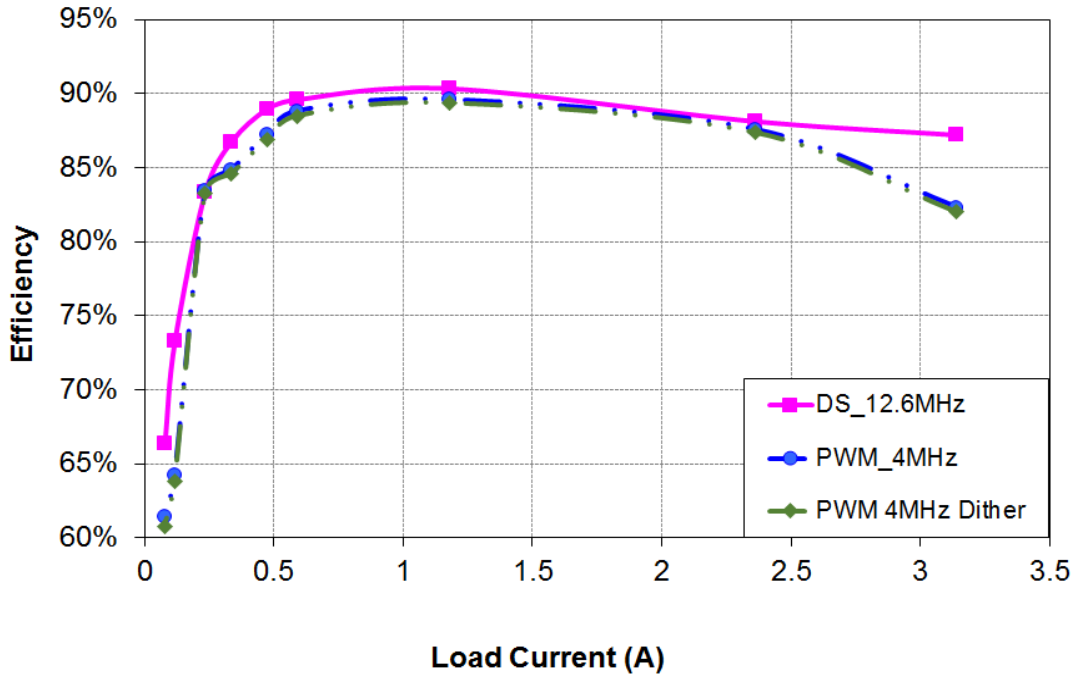


Fig. 12 Efficiency plot for the 4 MHz , dithered 4 MHz PWM and ΔΣ (DS) buck regulators. The F_{clk} of the ΔΣ regulator was 12.6 MHz.

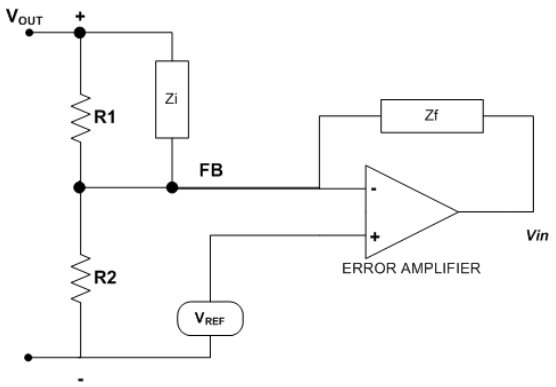
V. IMPACT OF LOAD CHANGE

From the previous sections, it is seen that the ΔΣ buck regulator shows the best performance in terms of spurious requirements of GSM system as well as power efficiency. To completely check the suitability of the ΔΣ controller, it is also necessary to examine the time domain response of the buck converter. The transient response is measured by step change in load, line and load regulation and ripple on the output voltage.

A. Stability Analysis

One of the key parameters that control the load step response of the buck regulator is its phase margin [41, 42] which can be obtained by performing a stability analysis on the system. The voltage mode buck regulator has two poles and a high frequency zero contributed by the LC filter described in Table 1. To compensate this, a proportional, integral and derivative (PID) compensation network is designed to provide phase boost near the double pole frequency as shown in Fig. 13a [4, 42]. The converter's overall loop transfer function can then be determined by multiplying the compensator network transfer function with the gain of the modulator which is the s-domain equivalent of STF from (2) and the LC filter, which is given by (7).

$$TF = \frac{Zf}{Zi} * STF * \frac{(1 + s * ESR * C_{OUT})}{1 + s * ESR * C_{OUT} + s^2 L1 * C_{OUT}} \tag{7}$$



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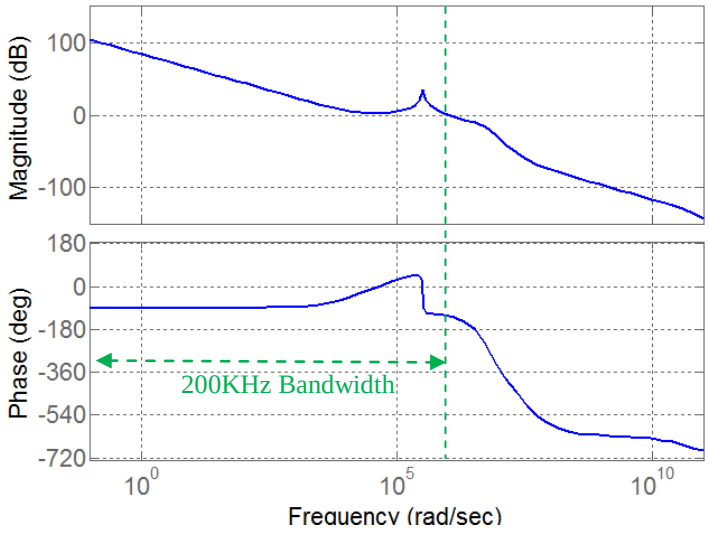


b)

Fig. 13 a) PID Compensation network for the buck regulator. b) Bode plot (Gain and Phase plot) of the over all transfer function for the ΔΣ buck regulator

The DC gain of the ΔΣ STF is given by the ratio of the constants b and a1 and is approximately equal to unity. Fig. 13b shows the Bode plot of the overall transfer function of the ΔΣ buck converter. The system has a crossover frequency at 200 KHz and a phase margin of 50 degrees. The phase margin can be improved by adjusting the R1, R2 and Zf components in the compensation loop.

1) Load Step Response:

Fig. 14 plots the response of the ΔΣ system for a load step of 150 mA to 2 A. The settling time of V_{OUT} is determined by the phase margin of the ΔΣ system [42]. The typical value for load regulation required in this application is 0.5% per Ampere [28, 29]. The ΔΣ buck regulator shows a load regulation of 0.3% per Ampere and therefore meets this requirement with sufficient margin. The simulated line regulation value was 0.1% for the V_{supply} ranging from 3 V to 5.5 V which is well within the standard requirement [28-30].

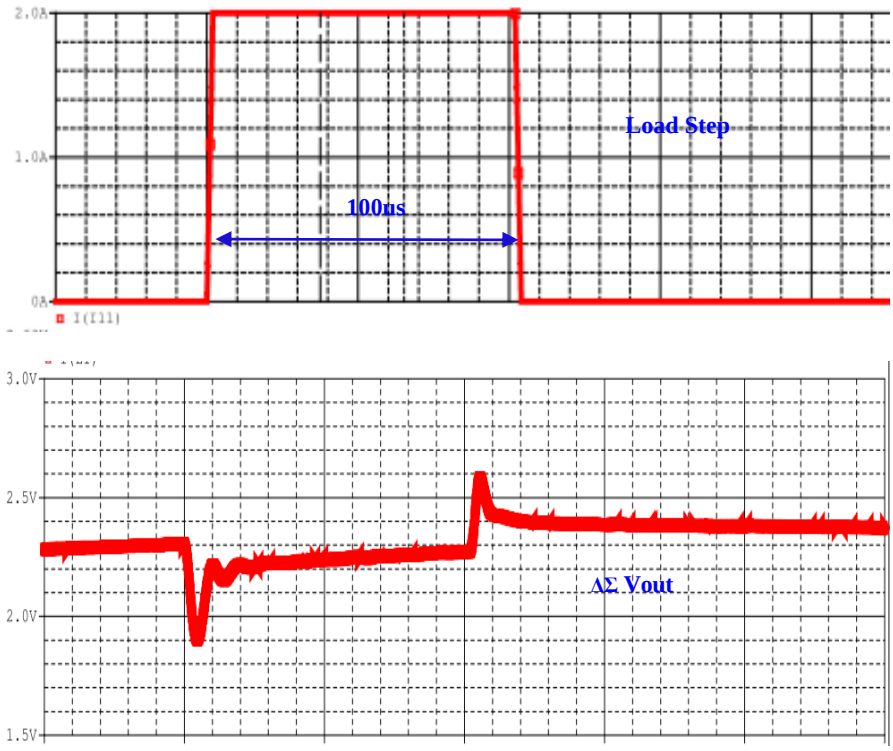


Fig. 14 Transient load step response of the 3rd order ΔΣ based buck regulator with OSR=32. F_{clk} =12.6 MHz was used for this test

2) Steady State Response:

Most DC-DC converters allow peak-to-peak ripple at the output to be less than 1% of its average value as a rule of thumb [4, 42]. For the V_{OUT} of 2.3 V, this corresponds to 23 mV. Since the ΔΣ modulator has random variation, it is necessary to measure the ripple voltage by looking at the V_{OUT} waveform over a longer time interval. Fig. 15 shows the V_{OUT} ripple of the ΔΣ buck converter with the inset showing the random variation of the ripple. This regulator shows a maximum peak to peak ripple of 6.5 mV, thus meeting the standard ripple specifications with sufficient margin.

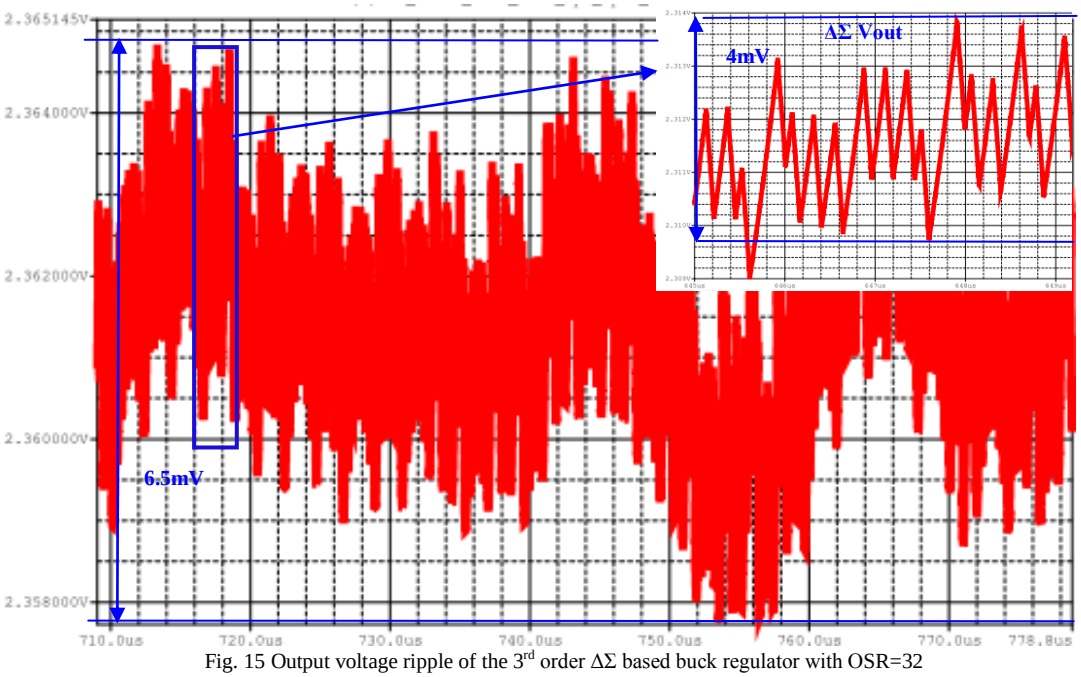
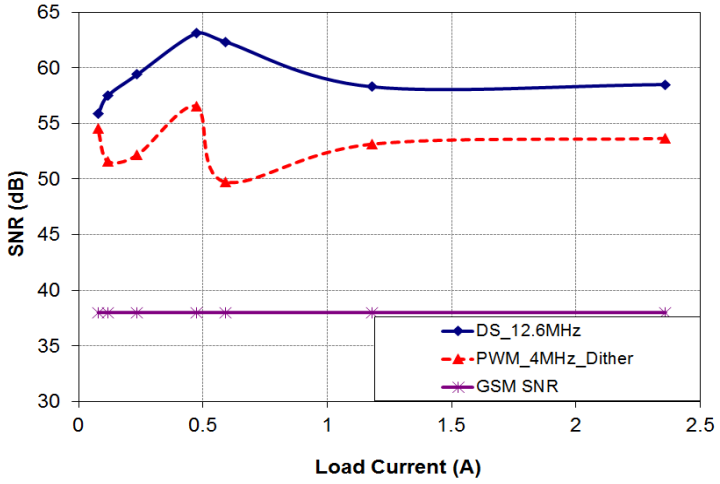


Fig. 15 Output voltage ripple of the 3rd order ΔΣ based buck regulator with OSR=32

Therefore the transient performance of the ΔΣ buck regulator meets the specifications required by a buck converter used in wireless systems.

B. Impact of Change in Load Current on Spurious Performance

In addition to the load regulation, different load currents also have a notable impact on the SNR and the spurs of the buck converters. The same test conditions of V_{supply} of 3.6 V, V_{OUT} of 2.3 V that were used in Section II were used in this study. Fig. 16a plots this effect on the SNR for the different load currents. As the load current increases, the noise floor also increases which causes the SNR to decrease. The GSM SNR requirement is also shown in the figure. It is seen that the SNR of the ΔΣ buck regulator meets the in-band prerequisite of the GSM system with more than sufficient margin. The SNR variation of the 20% dithered 4 MHz PWM buck regulator is also added in this plot. While both the regulators meet the SNR requirement specification, the SNR of the ΔΣ buck regulator is better than the PWM regulator with dither.



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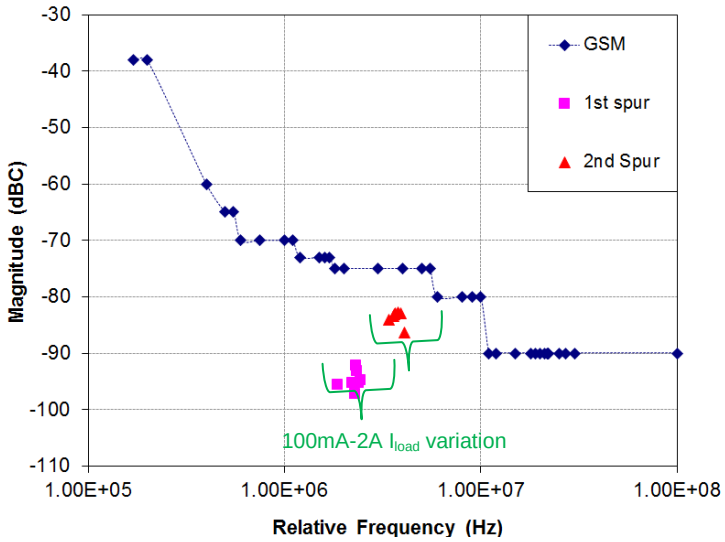


b)

Fig. 16 Spurious performance with load current variation a) Change in SNR b) Comparison of ΔΣ buck regulator's spurs against the GSM spectral mask

Change in the load current does not modify the switching frequency of the PWM buck regulator; as a result their spur magnitudes and frequencies remain constant for the different I_{load}. For the ΔΣ buck regulator, the variation in load current caused less than 6 dB change in spur magnitudes while the spur frequencies remained relatively constant.

Fig. 16b uses the above result and compares the spurs of the ΔΣ buck regulator obtained from the I_{load} variation from 100 mA to 2 A against the GSM spectral mask. From the figure it is seen that there is no significant change in the spurs of the ΔΣ buck regulator and it is still able to meet the GSM spectral conditions with more than 9 dB margin.

C. Dynamically Changing Load Application - Change in V_{OUT}

While the results from the previous section describe the performance of the buck regulators under steady state condition, it is also critical to examine their performances for loads that change dynamically. In wireless systems, the power amplifiers often consume the most power delivered by the battery thereby affecting its efficiency. One of the methods used to improve this efficiency is by using envelope tracking [43-46]. Fig. 17 illustrates how the power amplifier has lower efficiency when it is powered by a constant voltage when compared to power supply with envelope tracking [46]. As the signal of the amplifier varies, a constant power supply will cause efficiency loss due to the unused voltage range which is dissipated as heat in the system. In the envelope tracking method, the power amplifier's supply voltage is changed synchronously with the envelope of the RF signal that is amplifying [44-46]. This means that the buck regulator powering these power amplifiers should be able to adapt to dynamically changing V_{OUT}. V_{OUT} can typically change from 1 V to 4 V. This corresponds to +/- 44% from the steady state value of 2.3 V [44].

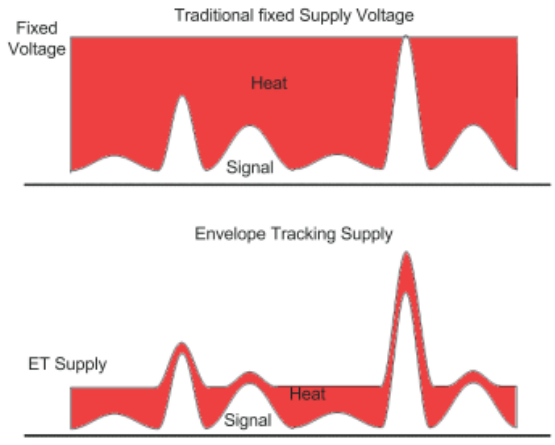


Fig. 17 Efficiency loss for power amplifiers used in wireless applications. A constant voltage supply vs envelope tracked power supply [45].

To determine the feasibility of the ΔΣ buck regulator for this application, the envelope tracking signal is used to vary the V_{REF} node in Fig. 1 [46]. This causes V_{OUT} to also vary proportionally. The tracking signal was modeled with a 0.1 V 20 KHz

sine signal super-imposed on the nominal 0.7 V dc voltage reference at the V_{REF} node. Although the actual tracking signal can consist of sine signals super–imposed with other step function signals, the sine signal was chosen as it emulates the general shape of the envelope tracking waveform in the simplest manner [46]. The amplitude causes the V_{OUT} to vary by +/- 13% of its set nominal value of 2.3 V.

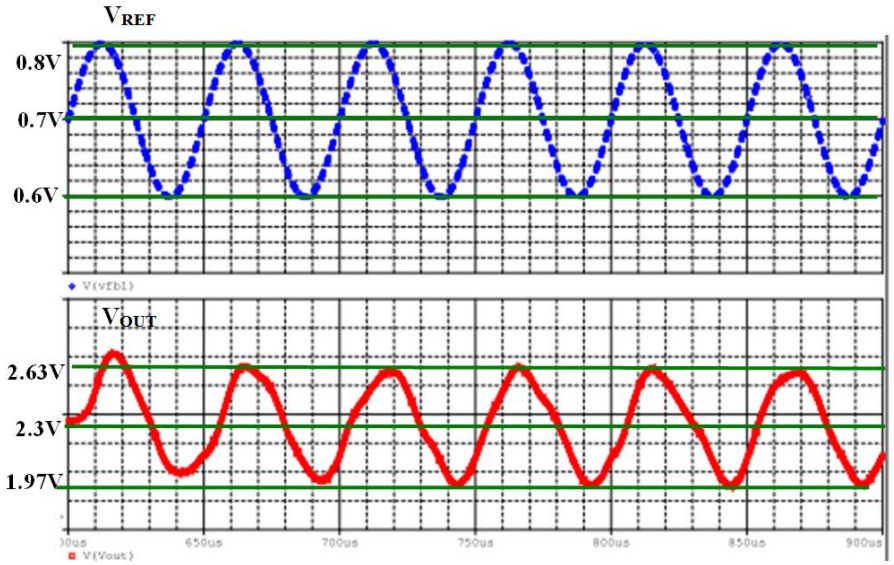
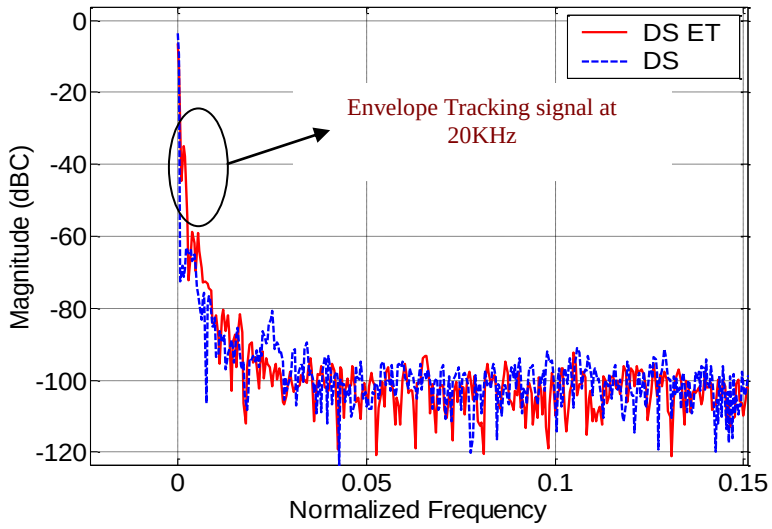


Fig. 18 Time domain response of the envelope tracking application

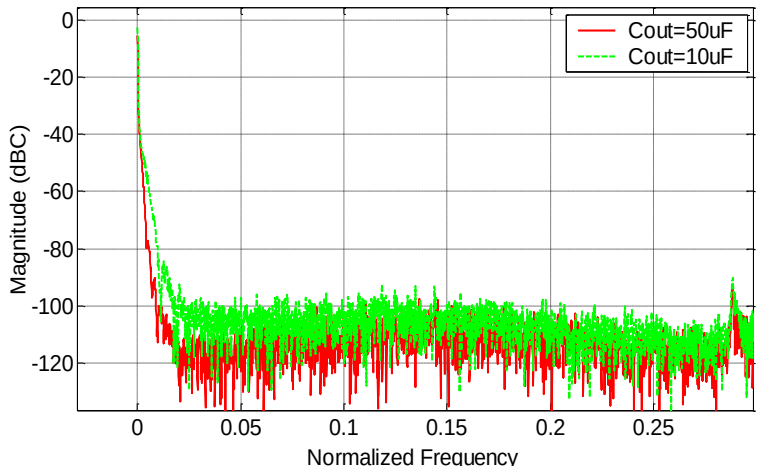
Fig. 18 plots the time domain response of the ΔΣ buck converter to the envelope tracking sine signal. For this simulation, V_{supply} of 5 V was used for a nominal V_{OUT} of 2.3 V. From the figure it is seen that as V_{REF} changes, the V_{OUT} also changes proportionately. Therefore, regulator is able to change its V_{OUT} in accordance with the tracking signal.

Fig. 19a compares the noise spectrums of the ΔΣ buck regulator with and without the envelope tracking sine input. Envelope tracking causes harmonic tones of the signal's fundamental frequency to be introduced in the in-band region. These tones increase the noise floor thereby reducing the SNR of the system. Despite the increase in noise floor, the ΔΣ buck regulator meets the in-band requirements of the GSM system with a SNR of 35.1 dB.

The SNR of the system can be enhanced by increasing the LC filter coefficients. A larger value output capacitor C_{out} reduces the V_{OUT} ripple and therefore improves the SNR. Fig. 19b compares the FFT spectrums of the ΔΣ buck regulator with C_{out} of 10 µF and with the C_{out} increased to 50 µF. This increase causes the SNR to improve by 4 dB and also reduce the spur magnitudes. Therefore for envelope tracking applications, it might be required to change the filter coefficients in order to meet the SNR requirements of the wireless systems. While this change can cause the system to have a slower transient response and decreased loop bandwidth it definitely improves the spurious performance of the buck regulator.



a)



b)

Fig. 19 Noise spectrum of buck regulators under envelope tracking (ET) condition
a) Comparison of a constant V_{OUT} with the envelope tracking ΔΣ buck regulator.
b) Comparison of the ΔΣ buck regulator with original with and larger C_{out} capacitors.

VI. CONCLUSION

Both good spurious performance and high efficiency are required by power supplies that power wireless systems. This paper shows that conventional PWM controlled switching regulators need to have a very high switching frequency at the expense of efficiency to meet the spectral requirements of different wireless standards. A substitute architecture using 3rd order ΔΣ modulator with OSR of 32 can meet the spectral requirement of GSM with 10 dB margin and shows 8% better efficiency than the PWM system running at the same clock frequency. While a 20% dithered 4 MHz PWM buck converter can meet the spectral requirement of the GSM system with 10 dB margin, it shows lower efficiency when compared to the ΔΣ buck regulator. The ΔΣ buck regulator meets the load change requirements such as stability, line and load regulation that are typically encountered by power supplies in wireless systems with sufficient margin. The feasibility of using the ΔΣ buck regulator for envelope tracking applications is also explored. For a 13% V_{OUT} change, the ΔΣ buck regulator can meet the spurious requirements of the GSM system. This work therefore shows that a ΔΣ buck regulator with its very good spurious performance and higher efficiency is a viable alternative for powering GSM system and other wireless standards.

ACKNOWLEDGEMENTS

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