# A FPGA-based Sequencer and Data Acquisition Electronics for CCD Detectors Management

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***Abstract*- This paper reports on the performances and characteristics of the Sequencer and Data Acquisition (SDAQ) electronics board developed at the Section of Astronomy and Space Science of Department of Physics and Astronomy of the University of Florence, a digital system able to control signals generation and data acquisition, mainly designed for new generation of CCD cameras, but also suitable to drive and acquire data from a large variety of solid state detectors. The SDAQ electronics design is in fact able to generate several digital LVDS signals useful for driving and controlling a solid state detector and some ancillary signals needed to perform analog to digital conversion on data and to perform on-fly data processing, like Correlated Double Sampling (CDS) at the same time. The SDAQ is also able to provide digital signals in order to control data acquisition by means of FPGA internally generated FIFOs and externally mounted static RAMs. Even RAMs are directly controlled by means of FPGA-generated digital signals.**

**Thanks to an external clock driver board and an analog to digital conversion and CDS board hosting the needed electronics components driven by SDAQ, it is possible to adapt, convert, and translate digital signal to TTL levels or other standard levels useful to drive detectors (e.g. CCDs analog phases or CMOS digital signals) and develop a stand-alone electronics system like a camera controller with some useful characteristics. Our electronics is in fact light, compact, and versatile as we were even able to drive a readout circuit developed to read very small currents (of the order of nA or hundreds of pA) generated by EUV-light driven photoelectric effect on Chemical Vapour Deposition (CVD) diamond film detector owning to its versatility.**

**With smart logic residing internally the SDAQ FPGA is based on several finite states machines written in VHDL language (VHSIC Hardware Description Language, where VHSIC means Very-High-Speed Integrated Circuits) and able to efficiently inter-communicate thanks to internal signals and logical ports. The VHDL code hosts several test benches in order to perform by itself some HW and SW checking on the overall SDAQ board, requiring a minimized external circuitry. By this way it is quite simple and relatively fast to perform tests even when the SDAQ is operative (e.g. when it is working inside a CCD camera controller mounted on a ground-based telescope facility). SDAQ's finite state machines are controlled by means of a FPGA-hosted decoder that is able to decode formatted command coming from the "outside world". Hereafter we will describe the characteristics of the SDAQ controller as well as the tests and the engineering management procedures performed by means of ours electronics facilities.**

***Keywords- FPGAs; CCD Detectors; Data Processing and Acquisition Electronics; Microcontrollers; RAM memories***

## I. INTRODUCTION

Nowadays there are a lot of application areas for CCDs in ground and space-based astrophysics [1] and earth observation, which could benefit from compact and versatile control electronics. These include imaging and spectroscopy from UV to IR, auto-guiding, star tracking and wavefront sensors for adaptive optics.

In particular, the high level of versatility and programmability allows a fast and reliable management of the CCD phases generation and data acquisition for several detector types and formats. The good level of integration is suitable for smaller controllers with reduced power consumptions and mass that permit their use in a large area of research fields, mainly for laboratory purposes and ground-based astronomy.

Moreover, with some modifications to get redundancies for space-reliability and to be compliant with the harsh space environment, it is possible for a versatile design to adapt to space-based astrophysics, by means of sub-orbital rockets and satellites hosting smart controllers for imaging cameras [2], [3].

Here, we describe a Sequencer and Data Acquisition board we developed in order to integrate the complete functionality of a dedicated programmable waveform generator with data acquisition capabilities and to provide both a CCD controller and a data acquisition system on the same board. Our design can implement waveform resolutions at a clock rate up to 100 MHz, implementing generation of control signals and fast data acquisition procedures.

It is designed specifically to provide programmable detector waveform generation and data acquisition management providing low circuit complexity and PCB circuit size and reduced power dissipation if compared to older DSP or general-purpose microprocessor-based design solutions. Thus, compacter and more lightweight cameras can be produced with the capability of programming any CCD waveform patterns, such as windowing and/or pixel binning and data acquisition algorithms.

As a consequence, the second generation SDAQ design could be derived by implementing its HDL code on a radiation hard device hosting redundant logic structures in a structured language paradigm, for applications related to sub-orbital or space experiments requiring CCD cameras.

The SDAQ electronics was originally designed and developed as a core controller for a new CCD camera for the CAOS spectrograph at the Catania Astrophysical Observatory [4], but it could be used as timing and control signal generator and data acquisition system for other kinds of sensors as diamond-based array UV/EUV detectors thanks to minor adjustments.

## II. THE SEQUENCER AND DATA ACQUISITION ELECTRONICS

The Sequencer and Data Acquisition electronics board [5] is logically structured in three sections:

- The SEQUENCER section, for detectors timing and control signal generation (e.g. for CDS – Correlated Double Sampling electronics boards);
- The DATA ACQUISITION section, to acquire and store digital data by RAMs memories from an external 16-bit resolution analogy to digital converter (ADC);
- The INTERFACE section, for communications with a PC or a laptop interfacing the board.

The SDAQ circuit is designed to manage the clock timing required by any detector based on an array of pixels (mainly a CCD sensor), the data acquisition procedures and I/F functions. Figure 1 shows a schematic diagram representing the SDAQ overall architecture. The dual function of this circuit is clearly shown in this diagram [6].

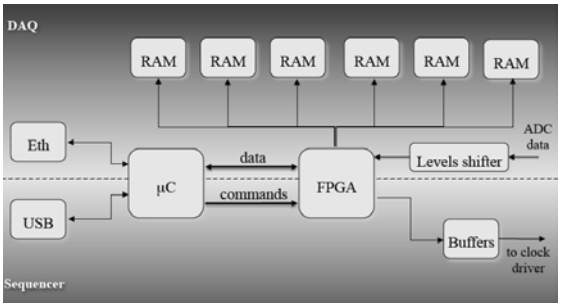


Figure 1 Block scheme of the SDAQ architecture

In order to accomplish such functions, we selected programmable components, as a FPGA (Field Programmable Gate Array) and a microcontroller (µC), supported by on-board PROM (not shown in Fig. 1, but visible in Fig. 2), six banks of RAM memories (6x16 Mbit Static RAM) and interfaced through Ethernet 10/100 Mbps or USB modules. While FPGA handles high frequency signals and data addressing and processing, the µC performs some high-level operations like communication I/F and commands management.

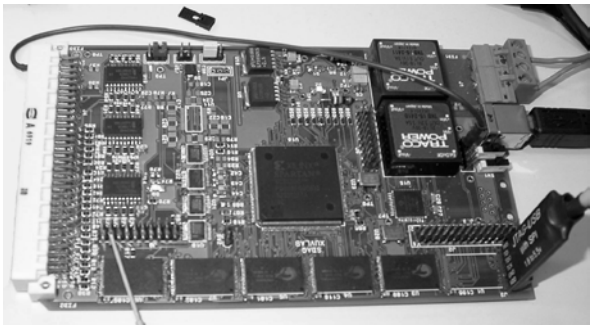

Figure 2 The SDAQ electronics hosted by a Euro card board (160 mm x 100mm)

The communication I/F is one of the µC tasks accomplished through the USB I/F or an Ethernet port by means of an external integrated module (XPORT module).

The DAQ system consists basically of a 12-MB SRAM controlled by the FPGA and acting as a large FIFO; this stores the 16-bits ADC data and waits for the request signal to send them to the µC. Then, the µC sends the data to the computer, through the USB port. The FPGA keeps the core program to operate the Sequencer and DAQ; its design meets the required level of versatility. Owing to the widely available resources and the capability of high-frequency operations (100 MHz clock) of this device, it is possible to implement a modular design, a high level of configurability and a high time resolution (10 ns).

Parameter configuration is not useful for CCD camera end users, but it is crucial for tests and optimization; therefore, some parameters are "frozen" after testing sessions. All the bias voltages necessary to supply the circuits are generated on-board (CMOS +3.3V and TTL +5V levels), requiring only a supply voltage ranging from 18V to 36V as input, thanks to two TRACO POWER DC-DC switching power converters. Other useful voltages like +1.2V and +2.5V are generated thanks to common voltage regulators integrated circuits hosted by the board.

The SDAQ board can be connected to a bus or a backplane board by means of a DIN 96-pin connector to assure an optimal and reliable mechanical and electrical interface. All the I/O signals are buffered by means of octal buffer line drivers (74HC244 IC); level shifting, allowing data transfer in a multi-voltage system, is performed through Maxim MAX3002 voltage level translators. The board can also mount a MAX3250 RS232 transceiver available for double serial lines if debug procedures or serial communication with other electronics systems is required.

### *A. The Sequencer*

The Sequencer is devoted to the generation of digital clocks to readout detectors [7]. It can be considered also as a Logic Board or Timing Circuit; its main task is to provide digital clocks to a Clock Driver, other digital signals like the Clamp and Sample to a Correlated Double Sampling circuit (CDS), and the Start Convert to drive the A/D conversion from an external board hosting an ADC.

Many detectors are available on the market; they differ from each other on numbers of pixels, size of sensitive area, numbers of read-out circuits and bias voltages; however, they are basically driven by digital signals that are adapted, buffered, and converted to the analog domain by means of a Clock Driver board.

Each of these detectors has to be driven properly; thus, it is necessary to define the Sequencer properties and functional philosophy. In particular, our design was developed to obtain high versatility and compactness, and at the same time, to accomplish all the requirements from new generation CCDs, with wide area or with a mosaic conception, using emergent technologies in the field of electronics. So, we decided to develop a timing circuit using one of the last generation of FPGA logic devices to implement a structured and versatile VHDL design.

Programmable logics, introduced by some manufacturers, make use of FLASH-programming technology. This allows for programming logic components quickly and on board by means of a specific cable (JTAG cable), reducing significantly the device development phase. The main features of our design are:

- flexibility: the component can be quickly and simply re-programmed by FLASH technology; to accomplish this task we use a 2Mbit PROM memory (Xilinx XCF02S) in boundary scan configuration;
- portability: the VHDL code can be quickly ported on a different device, even on a space qualified rad-hard device FPGA with some modifications;

- stability and reliability of clocks: once programmed, FPGAs acts as a not programmable hardware; therefore, it is unaffected by jitter noise;
- certified timings: programmable logics have maximum propagation delay times specified by the manufacturer. Moreover, after the implementation of a project, mutual delays between all pins can be firstly simulated and then verified and more than one error or warning report could be generated and consequently solved.

All the clocks and control signals (see Fig. 3 and Fig. 4) are driven by means of asynchronous finite state machines: the top-level interface microcontroller I/O ports owe its thanks to a 4 x 16 decoder. It decodes commands from the high level software GUI (Graphical User Interface) that interfaces the microcontroller firmware written in C language.

Actually, the VHDL project implemented in the FPGA Xilinx Spartan 3 XC3S200 model that we selected for our design is able to generate eight clocks and three control signals for a particular CCD sensor and readout electronics, the E2V-4240 detector with a frame format of 2048 x 2048 pixels, chosen for the CAOS spectrograph at the Catania Astrophysical Observatory.

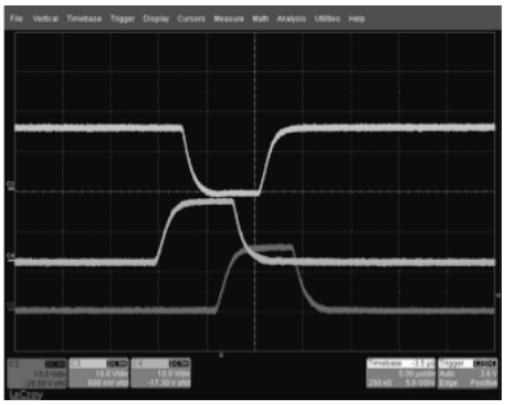

Figure 3 A set of E2V-4240 CCD vertical register clocks (vertical phases) generated by the Sequencer and shaped by means of a clock-driver electronics

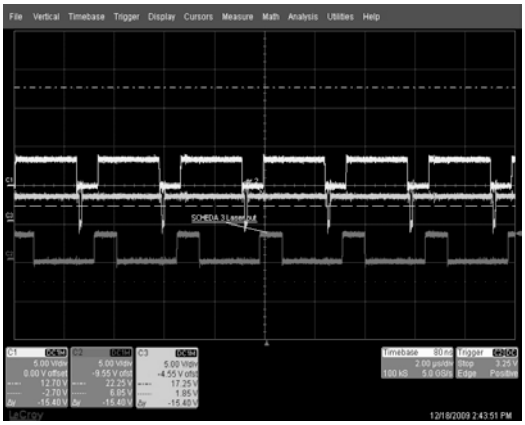

Figure 4 A set of control signals for the Correlated Double Sampling electronics board inside the CAOS CCD camera controller

Nevertheless, the SDAQ board is able to generate more phases and control signals in a structured manner designed by means of finite state machine algorithms controlling delays, glitch phenomena and buffering the clocks. In fact, the selected FPGA implements 200K system gates and 4320 logic cells and is provided by a large number of LVTTL compatible I/O pins (up to 173 I/O) thanks to its large package (208 pins).

All the developing and programming sequences are performed by means of freeware Xilinx web-pack ISE Design Suite in combination with Model Sim XE III (see Fig. 5), an integrated environment for design development as schematics or VHDL codes, necessary to simulate, route, and synthesize projects.

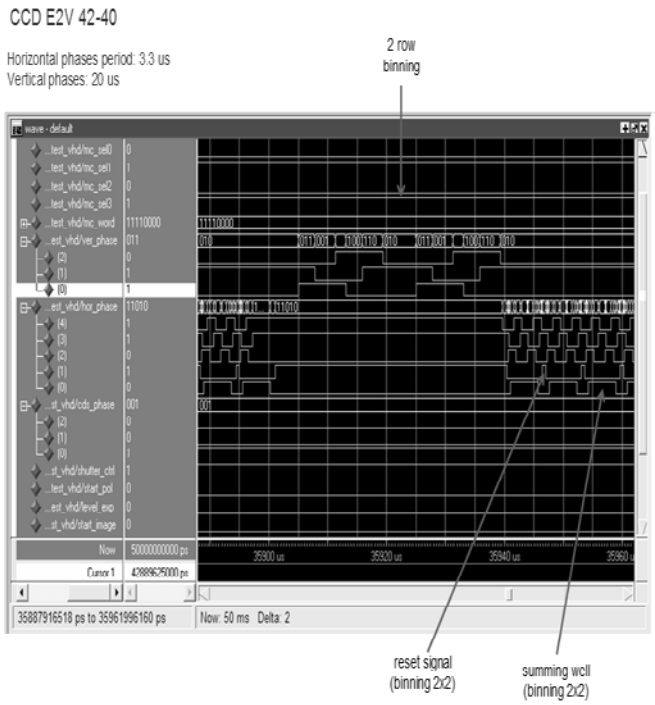


Figure 5 A typical ModelSim simulation session for E2V CCD-4240 horizontal and vertical phases with binning 2 x 2

The VHDL project is composed mainly of three blocks:

- the control logic functional block managing the operational modes like “test mode” for sequencer and DAQ testing and “setup mode”, e.g. for setting acquisition procedures and cleaning detector procedures;
- the phases/clocks and exposure time control block, generating control signals, horizontal and vertical phases and managing the exposure time and the shutter’s trigger;
- the communication interface block, interfacing microcontroller and managing commands from the high level SW interface.

In particular, the phase control block is very flexible because it is based on a parameterized phase generation code and on a counter section that numbers phases. So, it is possible to set up the phase duration (on multiples of base time) and the phase duty cycle owing to internal counters, and ultimately to set the number of phase periods. It is also possible to change quickly the base time thanks to an implemented clock divider block setting the reference time as multiple of the physical clock period.

### *B. The DAQ and the Interface to the Outside World*

The DAQ hardware interfaces digital signals to the PC. It could be realized by means of modules that could be connected to the computer ports (parallel, serial, USB, etc.) or cards connected to standard slots (PCI, ISA, etc.) into the PC motherboard.

Our design implements a stand-alone module that is connected to USB or Ethernet port and is able to send or receive data and commands to and from the high level SW

interface running on the PC-side. The data acquisition and processing flow, from the converter to the PC, is shown in Figure 6.

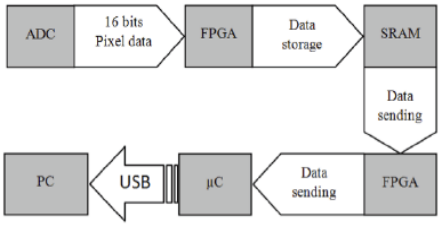


Figure 6 The Data acquisition and processing flow inside SDAQ board

Firstly, 16 bits/pixel format data are transferred to the FPGA and then to the SRAM memory buffer before being readout via a microcontroller interfacing FPGA. The DAQ internal logic is mainly composed of three parts:

- an input 2k x 16 bit FIFO (First In First Out) memory and its controller;
- a SRAM external memory controller;
- an output 2k x 16 bit FIFO memory and its controller.

FIFO memories are used as buffer memories between two asynchronous systems. In fact, they interface input data from an A/D converter (16 bit @ the 'start convert' signal frequency) and output data to the microcontroller. FIFO memories are implemented inside FPGA by means of the Xilinx CORE Generator, a useful tool for memory logic block generation and control. Their format and data depth can be simply parameterized before synthesizing the VHDL project; so we chose a 2k format for buffering a 2kpx CCD row (2048 px @ 16 bit) at a time.

The FIFOs and SRAM controllers characterize the DAQ core. The latter is capable to address 16-bit data through a bi-directional port by means of a signal for memory enabling and a 20-bit address. We chose this configuration to assure continuous data flow from the A/D converter to the microcontroller output at a rate fixed by the analog to digital conversion signal, generated by Sequencer and ranging the ADC characteristics (start convert signal).

The use of the bidirectional port is switched between SRAM memories input and output FIFOs. While input FIFO is continuously filled by incoming data, output FIFO is filled and emptied at a 2kpx (4kBytes) data rate packets. In fact, while microcontroller reads data already stored into the output FIFO, data flows directly from A/D converter to the SRAM blocks through the input FIFO. When the output FIFO is empty, the SRAM controller enables data reading from RAM, disabling data writing operation to RAM from input FIFO. So, the latter acts as a buffer memory, waiting for a new SRAM write cycle.

SRAM controller addresses data serially and manages memories altogether as a large FIFO, exploiting a dual set of HDL pointers for reading and writing procedures. Pointers are refreshed by means of two counters that act incrementing addresses for writing or reading the following memory location. In this way SRAM memories are managed by means of asynchronous signals with respect to the 100 MHz main clock; so, high frequency clock is only fed to the FPGA avoiding interference phenomena on the board.

## III. SDAQ FIRMWARE

The SDAQ electronics firmware (FW) includes the microcontroller FW and the FPGA FW (stored in a dedicated PROM and loaded to the FPGA at the board bootstrap).

### A. Microcontroller FW

The microcontroller FW was developed in C language under the CCS (Custom Computer Service Inc.) compiler in order to compile and link C files and header files to Assembler language. hex format.

It manages 16-bit data packets coming from the FPGA thanks to an 8 bit parallel port and other 8 standard I/Os and it transfers data packets to the high level SW via the USB integrated port endpoints as well receiving commands from the user. The same I/Os are used to set the integration time value to the FPGA, representing thus a 16-bit bidirectional port. FPGA Sequencer and DAQ sections can be reset by the user thanks to a dedicated command sent to the microcontroller that acts as an asynchronous reset.

It also exploits an XPORT module to interface the Ethernet network and to receive commands directly by LAN thanks to the TCP/IP protocol. The PIC18F4550 chosen microcontroller is fed by a 20 MHz external clock, mounted near the micro on the SDAQ PCB board.

### B. Fpga Fw

The low-level commands coming from the microcontroller are decoded by means of a simple 4x16 decoder interfacing the main Finite State Machine implemented inside the VHDL FPGA FW that acts as the brain of the sequencer and data acquisition system.

All the controlling finite state machines, decoders, counters, clock dividers, test benches, and configuration parameters are organized in separated VHDL files working in a structured environment managed by the Xilinx ISE Design Suite and ModelSim simulator.

Before synthesizing VHDL SDAQ projects, a test-bench-based simulation is ever performed by ModelSim to control and assure the optimized operating conditions of the overall design parts (see Figure 5).

## IV. THE GRAPHICAL USER IF

The high-level SW interface (see Figure 7 for a snapshot) was developed under the freely available NOKIA Qt Creator that allows the development of open source software governed by the GNU General Public License (GPL).


Figure 7 The high-level SW interface (GUI)

Qt Creator is a complete integrated development environment (IDE) able to create applications by means of the

Qt application framework. Qt is designed for developing applications and user interfaces once and deploying them across several desktop and mobile operating systems.

It includes:

- An advanced C++ code editor
- Integrated GUI layout and forms designer
- Project and build management tools
- Integrated, context-sensitive help system
- Visual debugger
- Rapid code navigation tools
- Supports multiple platforms (WinXP, VISTA, Windows 7, Linux, Mac)

The high-level SW interfaces the low-level SW via the USB microcontroller port. We used a simple FW up-loader (boot loader) through the USB interface and a graphical interface able to accelerate all the programming tasks.

The graphical interface is supported by multiple platforms, like Windows, UNIX, Linux and Mac operating systems by means of dedicated libraries and it is used to pass low-level commands to the microcontroller to acquire 16-bit data stored in SRAM memories. The acquired images data are then saved in the FITS format, a standard 16-bit format for astronomical images display and reduction.

Furthermore, it is possible to start and stop images acquisition sessions, to start detector-cleaning procedures, to reset the data acquisition system, and to set-up the exposure time and the image array size in pixels units.

## V. TESTS AND RESULTS

Within the test modality, two SDAQ operational modes are available: a “test mode” and a “setup mode”. The first mode allows the SDAQ for generating the signals checking the electronics and the general functions of the system once a specific detector and A/D converting electronics are selected. When the SDAQ is operated in “setup mode”, the parameters for the end-user application are fixed. However, some detector parameters are still configurable also after the controller setup (as exposure time, windowing, pixel binning, array dimensions, and pixel rate).

Within the test modality, it is possible to emulate a FPGA internal ADC, in order to auto-provide 16-bit data to the SDAQ acquisition section. Data values are generated sequentially from 0 to 65535 ADU (16 bit data) and fed by dedicated I/O pins to the input FIFO passing through the 96-pins DIN connector to fully simulate data from an external ADC. Then, they are acquired and transferred to the microcontroller and to the high level SW interface formatting it in a FITS image. The result is shown in Figure 8.

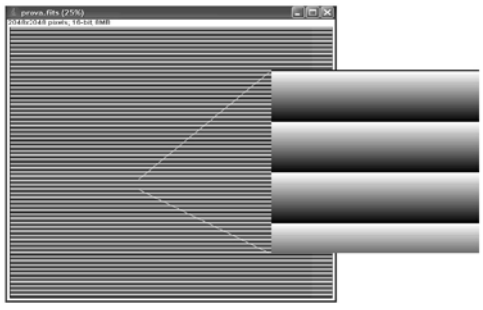

Figure 8 A 2048 x 2048 pixels image with shading bands representing 16 bit depth grey levels

Every image’s band showed in Fig. 8 represents 32 shaded rows (65536 grey levels divided by 2048 pixels) necessary to acquire 65536 grey levels stored in the same pixels number. This image, analyzed in details, guarantees the correct acquisition procedure by DAQ. It was tested properly up to an acquisition frequency of 5 MHz, showing always the same structures and characteristics. Moreover, the sequence of numbers representing data from the emulated ADC was checked on the images and on the board by means of a Tektronix TLA 601 state logic analyzer. Checks were performed thanks to some bit test points opportunely located on the board before input FIFO, between FPGA and SRAM memories and between microcontroller and FPGA.

All the control signals and phases generated by the sequencer were previously simulated and tested by means of a 1 GHz band-pass LeCroy Oscilloscope to check for timing characteristics and noise features (e.g. jitter). Phase and control signal counts and sequences were tested via logic state analyzer.

Finally, we performed some images of a test target with the E2V-4240 CCD and the electronic boards developed for the CAOS CCD camera to check the overall SDAQ operation inside the system, obtaining the results shown in Fig. 9. The image shows the overall 16 bits color depth and some sharp details, although the relay lens optics quality are not so good.

The laboratory tests reported an USB transfer rate to high level interface up to 600 KBytes/s and a total transfer time (including read-out of a 2048 × 2048 pixel CCD test image @ 300 kpixel/s) of 30 s.

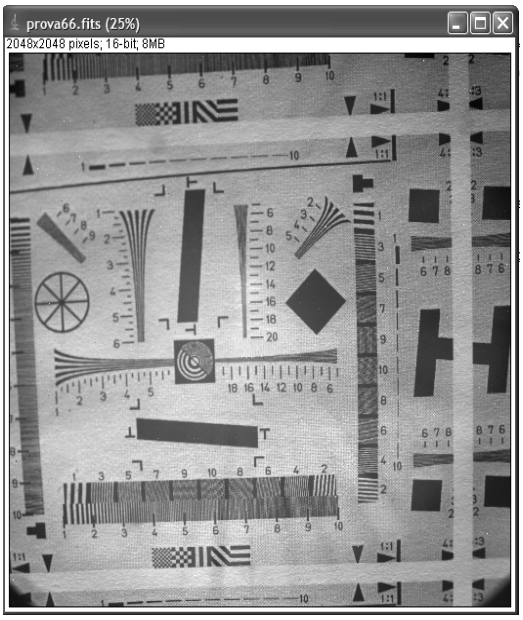


Figure 9 The test target acquired by the SDAQ board operating inside the CAOS CCD camera electronics

## VI. CONCLUSIONS

In this paper, we discussed the development of an innovative sequencer and data acquisition electronics based on a FPGA for a detector timing and signal processing, which is used mainly to manage not only CCD sensors, but also other kinds of solid state detectors too.

We also described the design of the SDAQ to drive detectors and to acquire their produced data. The overall electronics has been developed on a single board, integrating the functionality of a dedicated programmable waveform

generator with data acquisition capabilities based on a FPGA and a microcontroller.

A second-generation SDAQ design could be quickly produced, starting at the present, on a radiation-hard device implementing redundant logic structures in a structured hardware description language paradigm to work in a harsh radiation environment like space.

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