

A Simple Adaptive Control Technique for Shunt Active Power Filter Based on Clamped-Type Multilevel Inverters

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Abstract- The clamped-type multilevel inverters, which include Neutral Point Clamped (NPC) and Flying Capacitor (FC) inverters, are very attractive topologies for implementing shunt Active Power Filters (APF) in medium and high power networks. This paper presents a simple and adaptive control algorithm for a three-level current-controlled NPC-based APF. The proposed control algorithm employs three independent ADaptive LINEar combiners (ADALINE) modules to provide fast, accurate, and adaptive harmonic tracking. Two Proportional Integral (PI) controllers are implemented to generate the necessary reference current components for regulating the neutral point potential and the dc-side voltage, simultaneously. Furthermore, the proposed control algorithm is expanded for the control of the FC-based APF by replacing the Neutral Point (NP) potential controller with a modified dual band hysteresis current control (HCC) to regulate the voltage of the clamping capacitors using the redundant switching states. Simulation results are provided to evaluate the performance the two proposed multifunction control algorithms. The results expose the adaptive and accurate compensation of the load harmonics as well as the fast regulation of the voltages across the dc-side capacitors under normal and dynamic conditions.

Keywords- Active Power Filter; Flying Capacitor Multilevel Inverter; Harmonics Compensation; Neutral Point Clamped Inverter

I. INTRODUCTION

Active Power Filter (APF) has proven its capability to provide an effective, dynamic, and self-adaptive solution for the power quality problems. Different topologies have been proposed for the APF. One of the most popular topologies is the Shunt APF. It compensates the harmonic currents by acting as a controlled current source connected in parallel with the load. The Shunt APF injects the harmonic components of the load current but phase shifted by 180° so that the utility sees the load as if it was a linear load. The shunt APF merely consists of a power converter and a controller.

Two-level inverter is usually adequate for low power applications. Yet, due to the voltage and power ratings limitations of the power electronic switches, multilevel inverters configurations are being deployed in medium and high power applications. Multilevel inverters offer lower voltage stress per device. Additionally, multilevel inverters operate at lower switching frequencies and hence the switching losses and the electromagnetic interference are reduced. The most distinguished multilevel inverters topologies are the cascaded H-bridge inverters and the clamped-type inverters. The clamped-type multilevel inverters are divided to two main types; namely, the diode clamped inverter, also known as the Neutral Point Clamped (NPC), and the capacitor clamped inverter, which is also known as the Flying Capacitor (FC) [1]. Unlike the cascaded H-bridge inverter which requires multiple isolated dc links, the clamped-type inverters can be connected to a single dc-link. The beforehand mentioned advantage makes the clamped-type inverters economically preferable in spite of the increased number of clamping diodes required to implement a NPC inverter and the increased number of clamping capacitors required to implement a FC inverter.

In the three-level NPC inverter, the dc-side voltage is split into two by the use of two capacitors in series to provide the third output voltage level. The output may be connected to the Neutral Point (NP) between the two series capacitors through the clamping diodes. Thus, current is drawn from or to the NP causing one of the series capacitors to charge whilst the other discharge. Hence, the main disadvantage of the NPC topology is the need to control the NP potential [2-4]. Moreover, for an effective control of the NP, the total dc-side voltage has to be regulated at a constant reference value by adjusting the amount of real power absorbed by the inverter. Unlike the NPC inverter, the FC inverter does not need any control action to balance the NP potential; this is simply attributed to the fact that the NP does not play any role in the voltage clamping in the FC inverter configuration. In addition, the FC inverter has redundancies for switching states which can be used to control the clamping capacitor voltages. On the other side, the large numbers of capacitors used in the FC inverter are both expensive and bulky. However, the capacitors enable the inverter to ride through short duration outages and voltage sags [5].

The main function of the APF control algorithm is the calculations of the reference compensating currents need to be injected at the Point of Common Coupling (PCC) to compensate for the load current harmonics. Meanwhile, the controller should provide appropriate actions to regulate the dc-side potential. Various methods have been proposed to calculate the reference currents such as filtering through low pass and band pass filters [6], instantaneous reactive power theory [7-8], synchronous frame d-q method [9], power balance theory [10] and ADaptive LINEar combiner (ADALINE) [11-12]. The use of fixed frequency filters to separate the harmonics

and hence generate the reference currents introduces delays and frequency drifts in the system which affects the dynamic performance of the APF. The instantaneous reactive power theory requires complex calculations and it is sensitive to the supply characteristics. The power balance concept does not alleviate the need of another complementary method for harmonics identification. On the other hand, the use of ADALINE in the estimation of the reference currents yields better performance, more accuracy, and faster response^[13]. Meanwhile, it abolishes the problems attributed to other methods such as response time delays and sensitivity to supply waveform distortion.

The most widely used modulation technique is the Space Vector Modulation (SVM)^[14-15]. Although SVPWM can control the NP potential inherently as a part of the control procedures, still it is a complex voltage control technique that requires a lot of calculations. Moreover the control command in the SVM is a voltage vector while the proposed APF implements a current control philosophy. This means that more calculations are needed to convert the harmonics current compensation command into a voltage command before passing it to the SVM technique. The Hysteresis Current Control (HCC) is a competitive current control technique for the proposed APF. Its simple construction, fast dynamic and bounded error response^[16-17], along with the fact that it has a current command made it viable for the proposed application.

This paper presnets a simple adaptive control technique for APFs based on three-level current-controlled clamped-type multilevel inverters. The proposed control algorithm employs three independent ADALINE modules, one module per phase, to provide fast, accurate, and adaptive harmonic tracking. Proportional Integral (PI) controllers are used to generate the necessary reference current components for regulating the dc-side voltage of the multilevel inverter and the NP potential of the NPC inverter. A dual band HCC is utilized to generate the inverter gating signals needed to track the assembled reference compensating current. Furthermore, the proposed control algorithm is expanded for the control of the FC-based APF by eliminating the NP potential control loop and modifying the HCC to regulate the voltage of the clamping capacitors using redundant switching states. The performance of the proposed system is examined using the PSCAD/EMTDC program. The paper is organized as follows. The clamped-type multilevel inverters based APF configuration is described in Section II. The proposed control algorithms for the APF based on NPC and FC multilevel inverters are presented in Section III and Section IV, respectively. The simulation results are illustrated in Section V. Finally, Section VI concludes the paper.

II. APF BASED ON CLAMPED-TYPE MULTILEVEL INVERTERS

Fig. 1 shows the power circuit configuration of the proposed APF based on NPC inverter. It consists of a three-phase, three-level NPC inverter connected to the PCC, in shunt with a non-linear load; for instance, a three-phase rectifier. The load currents i_{la} , i_{lb} , i_{lc} are the sum of the APF compensation currents i_{ca} , i_{cb} , i_{cc} and the supply currents i_{sa} , i_{sb} , i_{sc} . The injected compensation currents track the load currents harmonic components. Accordingly, the supply current consists of the fundamental component only.

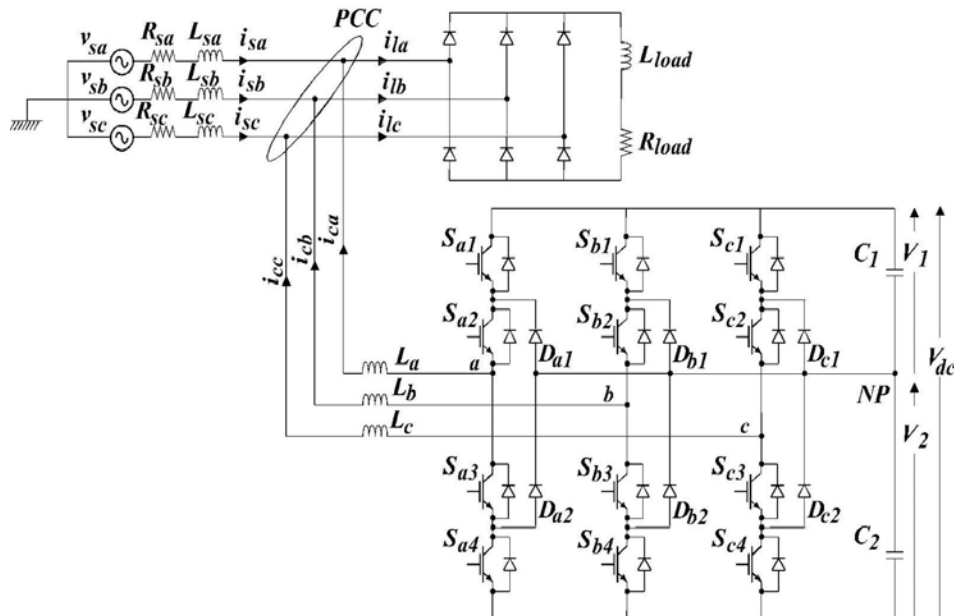


Fig. 1 Power circuit configuration of the proposed APF based on NPC inverter

Three inductors, L_a , L_b and L_c , are used for connecting the NPC inverter to the PCC for filtering of high ripples and smoothing. These inductors allow the APF to act as a controlled current source with respect to the power system. Similarly, Fig. 2 portrays the three-level FC-based APF. The only difference between the two topologies is that the clamping diodes, D_{a1} , D_{a2} , D_{b1} , D_{b2} , D_{c1} , and D_{c2} , are replaced with the three clamping capacitors, C_3 .

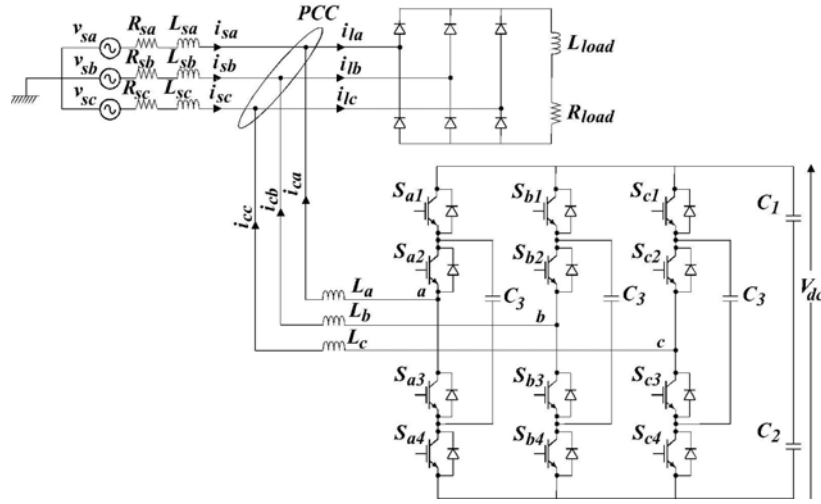


Fig. 2 Power circuit configuration of the proposed three-level FC-based APF

III. THE PROPOSED CONTROL ALGORITHM FOR THE APF BASED ON NPC INVERTER

The proposed control algorithm is simple, succinct, and easy to implement. Fig. 3 shows the block diagram of the overall proposed control algorithm. It calculates the required load harmonics compensation currents i_{cah} , i_{cbh} , and i_{cch} , the dc voltage regulating currents i_{cad} , i_{cbd} , and i_{ccd} , and the NP potential controlling current i_{cn} . The reference compensating currents, i_{ca}^* , i_{cb}^* and i_{cc}^* , are the summations of these components. A double band HCC is used to generate the gating signals needed to force the NPC inverter to track the reference compensating currents. It is worth mentioning that the proposed control algorithm can be realized with a reduced computational effort, hence, it is easy to implement. The details of each part of the proposed control system, shown in Fig. 3, are presented in the next subsections.

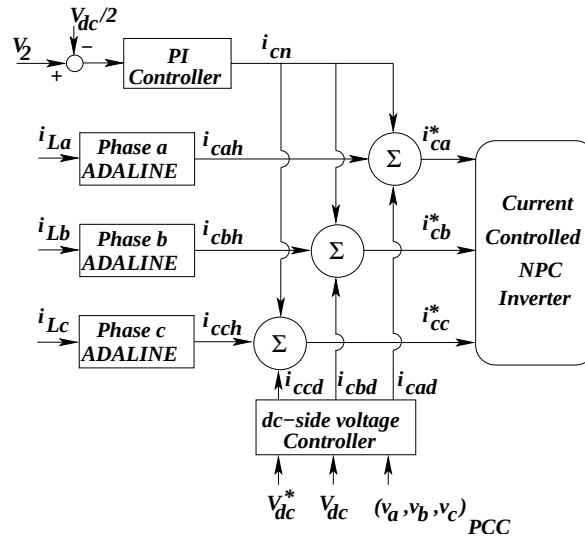


Fig. 3 Block diagram of the proposed control algorithm for the NPC-based APF

A. ADALINE Based Harmonics Identification

The effectiveness of APF operation depends on its ability to track the harmonics. Moreover, good harmonics tracking cannot be achieved without good harmonics identification. The use of ADALINE allows for excellent dynamic and self-adaptive identification of the load current harmonics. Its simple structure makes it easy to implement. The load current is expressed by Fourier analysis as follows:

$$i_1(k) = \sum_{n=1,3,\dots,N} I_{n1} \cos(2\pi nk / N_s) + I_{n2} \sin(2\pi nk / N_s) \quad (1)$$

where I_{n1} and I_{n2} are the amplitudes of the cosine and sine components of the n^{th} order load current harmonic, k is the sampling order and $N_s = f_s / f_0$ is the sample rate which is the ratio of the sampling frequency, f_s , to the nominal power system frequency, f_0 .

The input to the ADALINE is a vector $\mathbf{X}(k)$ consists of the cosine and sine terms resulting from the Fourier analysis of the load current. The unknown amplitudes of the cosine and sine harmonics components are combined in a weight vector, $\mathbf{W}(k)$. The input vector is multiplied by the ADALINE weight vector $\mathbf{W}^T(k)$ to get the estimated load current, $\hat{i}_l(k)$, as follows:

$$\hat{i}_l(k) = \mathbf{W}^T(k) \cdot \mathbf{X}(k) \quad (2)$$

where,

$$\mathbf{X}^T(k) = [\cos(\frac{2\pi k}{N_s}) \quad \sin(\frac{2\pi k}{N_s}) \quad \cdots \quad \cos N(\frac{2\pi k}{N_s}) \quad \sin N(\frac{2\pi k}{N_s})] \quad (3)$$

And

$$\mathbf{W}^T(k) = [I_{11} \quad I_{12} \quad \cdots \quad I_{N1} \quad I_{N2}] \quad (4)$$

The ADALINE weight vector $\mathbf{W}^T$ is adapted using the WIDROW-HOFF ^[18] learning rule which provides the least mean square error between the estimated load current and the actual one. For the k^{th} sampling time the WIDROW-HOFF rule can be written as follows:

$$\mathbf{W}(k) = \mathbf{W}(k-1) + \alpha \frac{e(k-1) \cdot \mathbf{X}(k-1)}{\mathbf{X}^T(k-1) \cdot \mathbf{X}(k-1)} \quad (5)$$

where $e(k-1) = i_l(k-1) - \hat{i}_l(k-1)$ is the prediction error and α is the learning parameter.

Decreasing the learning factor α decreases the prediction error, but at the expense of increasing the convergence time. On the other hand, increasing α increases the prediction error dramatically and decreases the convergence time. Therefore, there is a trade-off in selecting the value of α to get fast convergence, and hence fast response, with minimum prediction error. The most common approach to determine its value relies on trial and error ^[19]. The perfect learning is accomplished when the estimated load current is equal to the actual one.

Equations (2) to (5) demonstrate the ability to interpret the weights of the ADALINE; as the weight vector represents the magnitude of the different components. For instance, the instantaneous value of fundamental component of the load current, i_{l1} , is written as

$$i_{l1} = \sqrt{I_{11}^2 + I_{12}^2} * \sin(2\pi f_0 t + \tan^{-1}(I_{11} / I_{12})) \quad (6)$$

Accordingly, by subtracting the estimated fundamental component from the actual load current, the reference load harmonics compensating currents, i_{cah} , i_{cbh} , and i_{ch} , of the APF are obtained. These reference currents are fed to the current controller to inject the necessary harmonics compensation current component.

B. NP Potential Compensation

The control of the NP potential is a mandatory condition for a proper operation of the NPC inverter. Failure to meet this requirement will lead to an increased voltage stress on the semiconductor switches which in turn lead to the breakdown of these switches. Moreover, the fluctuation of the neutral point potential may lead to a distorted output current waveform. The use of auxiliary circuit to control the NP potential has been investigated ^[4]. However, due to the additional costs and power losses, this solution is generally not acceptable. The addition of an equal dc offset to each of the three-phase reference load harmonics compensation currents has been proven to be an effective and simple method to control the NP potential ^[2]. The added dc offsets forces the NPC inverter to inject a small dc current component in each of the three phases, which when added together cancel the average current flowing in or out of the NP and hence restore balance between the two capacitor voltages. However, this method is very sensitive to the modulation index. Low pass filters were investigated to produce the necessary offset ^[20-21]. However, this type of NP potential compensation introduces delays in the control system.

A simple PI controller is used to produce the necessary dc offset for the compensation of the NP potential. The difference between the two capacitor voltages represents the error in the NP potential. Thus a PI controller, with this error as its input, gives the dc offset needed to make the error equal to zero and hence compensate the NP potential. The difference between V_2 and $V_{dc}/2$ is introduced to a PI controller and the output is used as the reference NP potential controlling current component, i_{cn} . The error in the NP potential is expressed as the difference between V_2 and $V_{dc}/2$ rather than the difference between V_1 and V_2 in order to reduce the number of measuring points required.

C. DC-Side Voltage Control

The control of the NP potential is ineffective without a constant dc-side voltage. The control of the dc-side voltage is achieved via the compensation of the real power consumed in the inverter losses^[20]. Fig. 4 shows the proposed control algorithm to realize a constant dc-side voltage. A PI controller is used to regulate the dc-side voltage at a set value, V_{dc}^* . A digital synchronizing Phase Locked Loop (PLL) circuit, having the voltages at the PCC as its input is used to give unity sinusoidal waveforms at the fundamental frequency and in phase with the PCCs voltages. The output of the PI controller is multiplied by the unit waveforms obtained from the PLL circuit. The resultant is the sinusoidal reference dc voltage regulating currents components i_{cad} , i_{cbd} , and i_{ccd} . This component is in phase with the PCC voltage and hence it is capable of controlling the active power consumption by the APF and eliminating the error between the dc-side voltage and its set value.

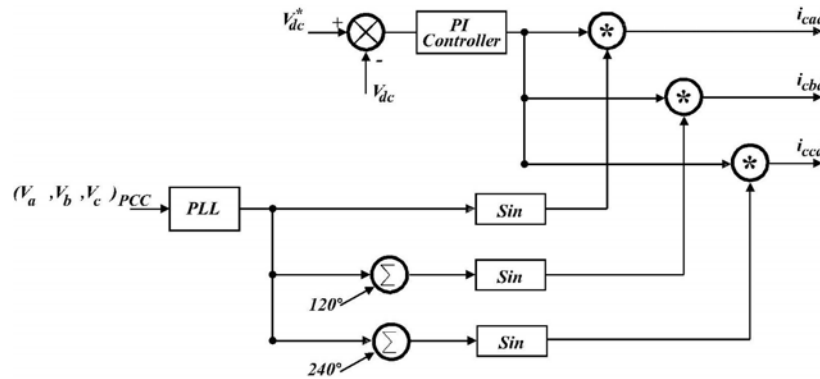


Fig. 4 Block diagram of dc-side voltage control

D. Hysteresis Current Control

The three-level NPC inverter has three possible phase leg outputs ($V_{dc}/2$, 0, and $-V_{dc}/2$). Accordingly, assuming positive phase current polarity, to decrease the actual compensating current, one of two possible inverter phase leg outputs (0, $-V_{dc}/2$) must be chosen. Likewise, to increase the actual compensating current, one of two possible inverter phase leg output ($V_{dc}/2$, 0) must be chosen. The simplest solution to make the controller self-dependent in taking these choices is to define two-offset-hysteresis bands as shown in Fig. 5. The upper hysteresis band represents the switching between the two adjacent voltage levels (0, $-V_{dc}/2$) and in such case the choice of zero output voltage increases the actual compensating current (Low boundary hit). Whereas the lower band represents the switching between the two adjacent voltage levels ($V_{dc}/2$, 0) and in such case the choice of zero output voltage decreases the actual compensating current (High boundary hit).

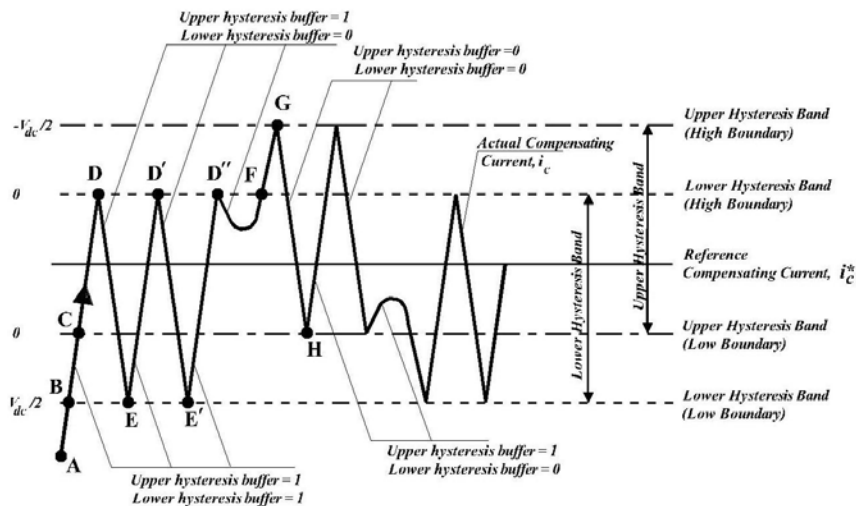


Fig. 5 Upper and lower hysteresis bands

Fig. 6 shows the block diagram of the proposed current control technique for Phase *a*, where the difference between the reference compensating current and the actual one is processed by two hysteresis buffers representing the upper and lower hysteresis bands, respectively. When the input signal exceeds the hysteresis buffer upper limit, the hysteresis buffer generates a logical one. When the input signal goes below the hysteresis buffer lower limit, the hysteresis buffer generates a logical zero. Each hysteresis buffer maintains the previous output level as long as the error current signal is inside the hysteresis band. The two logic outputs of the hysteresis buffers, upper and lower, are combined together and used as logic inputs to determine the gating signals per phase according to the switching states given in Table I.

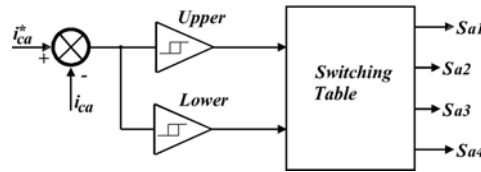


Fig. 6 Block diagram of the proposed current controller for the NPC-based APF

TABLE I SWITCHING STATES OF DOUBLE BAND HCC FOR THE NPC-BASED APF

Input (Upper : Lower)	Output voltage	Sa1	Sa2	Sa3	Sa4
00	$-V_{dc}/2$	0	0	1	1
01 or 10	0	0	1	1	0
11	$V_{dc}/2$	1	1	0	0

The operation of the proposed HCC and the transition between the different available voltage levels can be explained as shown on Fig. 5. At Point (A), the actual compensating current, i_c , is lower than the reference compensating current, i_c^* i.e. the current error is positive and greater than both hysteresis buffers upper limits. Therefore, the outputs of both hysteresis buffers are equal to one and a voltage of $V_{dc}/2$ is applied. As the actual compensating current increases it passes through Points (B) and (C) where no change occurs in the output of the hysteresis buffer. At Point (D), the error signal falls below lower hysteresis buffer's lower limit, therefore the lower hysteresis buffer's output changes to 0; this in turn changes the applied voltage to 0. As the voltage output is sufficient to force the actual compensating current down till it reaches Point (E) or (E'), respectively. The second case is as the one shown at Point (D''), where the change of the voltage level to 0 is not enough to force the actual compensating back down within the lower hysteresis band and the actual compensating current continues to increase till it hits the upper hysteresis band's high boundary at Point (G). At Point (G) the actual compensating current starts to exceed the upper hysteresis band's high boundary i.e. the error signal falls below the upper hysteresis buffer lower limit, therefore the upper hysteresis buffer's output is changed to 0; and so this changes the output to $-V_{dc}/2$.

IV. EXTENSION OF THE PROPOSED CONTROL ALGORITHM TO CONTROL A FC-BASED APF

The proposed control algorithm, described in Section III, can be easily adapted and extended for the control of the FC-based APFs. Fig. 7 shows the block diagram of the proposed control algorithm after adaptation to suit the control purposes of the FC-based APF. The adapted control algorithm performs the two main control functions required for the APF operation.

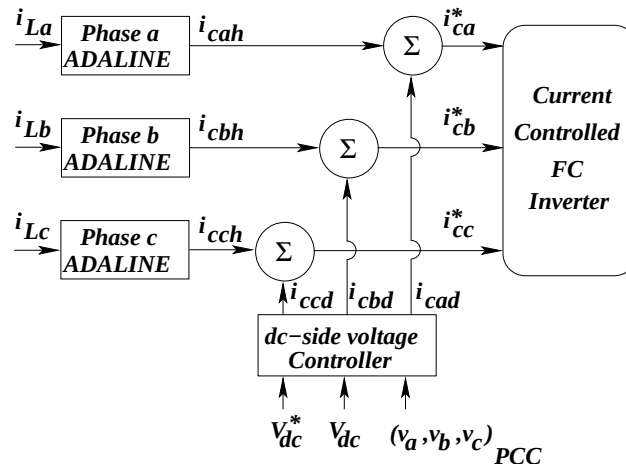


Fig. 7 Block diagram of the proposed control algorithm for the FC-based APF

The reference compensation currents of the FC-based APF consist of two components only. The first component is known as the reference load harmonics compensation current, i_{cah} , i_{cbh} and i_{cch} . This component is responsible for tracking the load side harmonics. The calculation of these components is performed through the use of three independent ADALINE modules, one per each phase, as described in Subsection III.A. The second component is the dc voltage regulating current component, i_{cad} , i_{cbd} and i_{ccd} . This component is responsible for adjusting the amount of real power absorbed by the APF to be equal to the power lost in the inverter switches. These components are calculated through a simple PI controller in the same manner described earlier in Subsection III.C. The summation of these two components together constitutes the reference compensating currents i_{ca}^* , i_{cb}^* and i_{cc}^* . The reference compensating currents are then passed to the HCC which performs the current control of the FC inverter, controlling in the same time the clamping capacitor voltages.

The use of capacitors for phase voltage clamping in the FC inverter, instead of diodes as in the NPC inverter, permits several

redundant switching combinations for a particular phase voltage level generation. These redundant switching combinations are used for controlling the charging and discharging of the clamping capacitors [22]. As a result, the proposed current control algorithm, for the three-level FC-based APF, inherently balances the voltages of the clamping capacitors by using the beforehand mentioned redundant switching states.

The dual band HCC, described in subsection III.D, is used; however it is modified to allow for the clamping capacitor voltage control as a part of the current control. Fig. 8 shows the block diagram of the modified current control switching scheme for the three-level FC inverter. The difference between the reference compensating current, i_c^* , and the actual one, i_c , is processed by two hysteresis buffers. The output of the upper and lower hysteresis buffers, Up and Lo, along with the sign of the compensating current, the dc -side voltage, and the clamping capacitor voltage are used to determine the gating signals according to the switching states given in Table II. The two redundant states available to produce zero output phase voltage (01 or 10) are used to keep the clamping capacitor voltage at its desired level, $V_{dc}/2$.

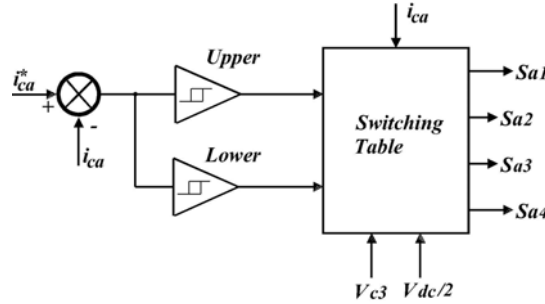


Fig. 8 Block diagram of the proposed current control switching scheme for clamping capacitor voltage control

TABLE II SWITCHING STATES OF DOUBLE BAND HCC FOR THE FC-BASED APF

Input Up:Lo	i_c	$v_{c3} - v_{dc}/2$	Output voltage	Sa1	Sa2	Sa3	Sa4
00	+/-	+/-	$-V_{dc}/2$	0	0	1	1
01 or 10	+	+	0	0	1	0	1
	+	-	0	1	0	1	0
	-	+	0	1	0	1	0
	-	-	0	0	1	0	1
11	+/-	+/-	$V_{dc}/2$	1	1	0	0

V. RESULTS

The performance of the proposed control algorithm is examined by simulation using the PSCAD/EMTDC program. The sampling time is set to 0.1 millisecond. It was found that the value of the learning factor that gives the best harmonics tracking performance is 0.1. The upper and lower hysteresis bands are adjusted at 3% and 6% of the maximum value of the compensation current, respectively. Three different study cases are presented to evaluate the operation of the proposed APFs under different voltage levels in distribution networks.

A. Case 1: NPC-Based APF to Compensate for Low Voltage Rectifier Load

In this study case, the non-linear load is a rectifier feeding an inductive load. The circuit parameters of the system under study, shown in Fig. 1, are given in Appendix A. To examine the dynamic performance of the proposed control algorithm, the non-linear load is suddenly increased at $t = 0.15s$ and reduced at $t = 0.25$.

Fig. 9(a) and Fig. 9(b) show the PCC voltage and the supply current of phase a , respectively, while the corresponding load current is traced in Fig. 9(c) during the load changes. The supply current remains sinusoidal before and after the load variation. The THD of the supply current is 3.9% which complies with the allowable harmonics limits [23]. Fig. 10 portrays a zoom from Fig. 9 at the instant when the load is increased. It is clear that the supply current is in phase with the PCC voltage even during the dynamic change. This is not surprising since the displacement factor of the load current is unity which means that compensating harmonics leads to a unity power factor at the PCC.

To demonstrate the ability of the adopted current controller to track the reference current, Fig. 11(a) and Fig. 11(b) illustrate the reference and actual compensating currents of phase a , respectively. Fast current tracking with a tight error is obvious. This current waveform carries the information for compensating load harmonics, regulating the dc -side voltage, and balancing the NP potential.

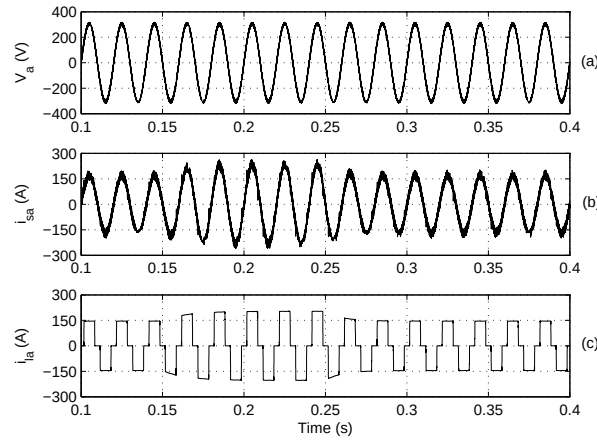


Fig. 9 Harmonics compensation of a rectifier load:
(a) PCC voltage, (b) supply current, and (c) load current

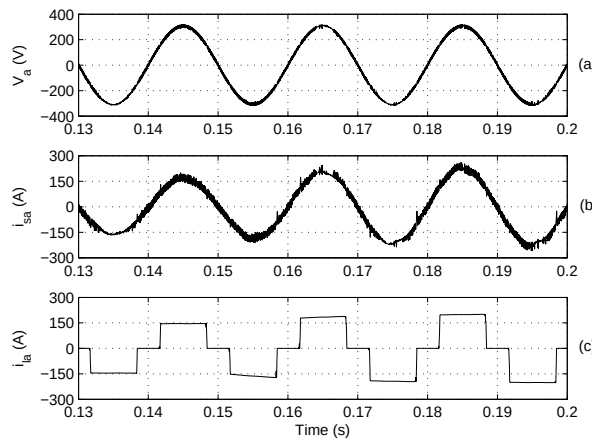


Fig. 10 Zoom from Fig. 9

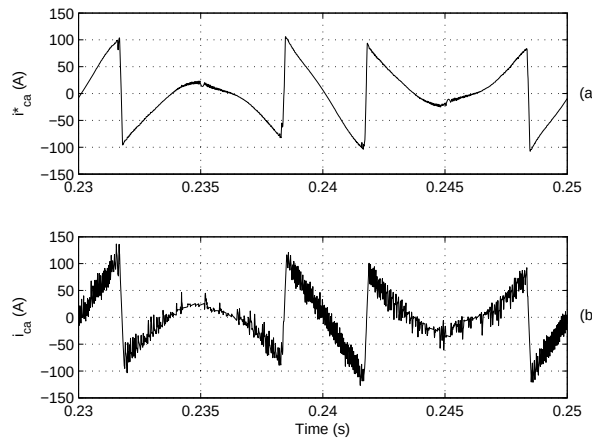


Fig. 11 Phase a reference and actual compensating currents

The performance of the dc-side voltage controllers for regulating the dc voltage and balancing the NP potential are investigated in Fig. 12. Fig. 12(a) portrays the dc-side voltage. When the load is suddenly increased, a dip of 3.4% occurs at the dc-side voltage and duration of two power cycles. Reducing the load to its initial value causes the dc-side voltage to rise by 4.5% with the same duration of the dip. This test result evaluates the disturbance rejection capabilities of the proposed simple PI controllers which are accepted for the APF application. During the steady-state operation, the deviation of the dc-side voltage from the reference value is less than 1.5%. The voltages across the dc-side capacitors C_1 and C_2 are illustrated in Fig. 12(b) and Fig. 12(c), respectively. Fig. 12(d) depicts the percentage NP potential unbalance (NPU) which is the ratio of the voltage difference between the dc-side capacitors to their average value and is given by

$$\%NPU = \frac{V_1 - V_2}{(V_1 + V_2)/2} \times 100 \quad (7)$$

The voltage variation between the two capacitors is less than 2% which demonstrates the ability of the proposed control algorithm, for the NPC-based APF, to maintain a constant dc-side voltage and to control the NP potential in addition to the precise harmonics compensation.

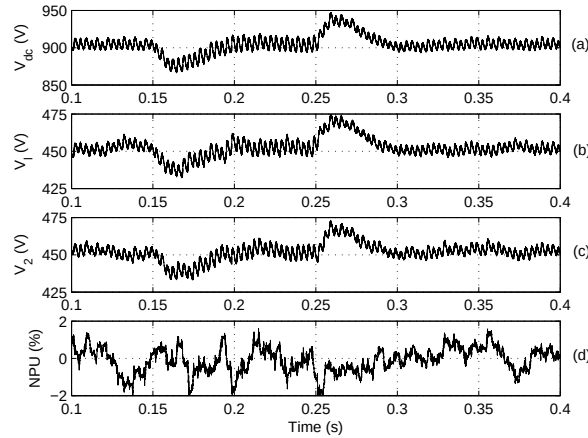


Fig. 12 Performance evaluation of the dc-side voltage controllers: (a) dc-side voltage, (b) voltage across C_1 , (c) voltage across C_2 , and (d) percentage NP voltage unbalance

B. Case 2: NPC-Based APF to Compensate for Medium Voltage Controlled Rectifier Load

This study case presents the operation and performance of the proposed NPC-based APF in medium voltage level. The uncontrolled rectifier, used in the previous study case, is replaced by a controlled rectifier operating at different firing angles. Simulation parameters of this study case are given in Appendix B. The APF is activated at 0.1s where the firing angle of the non-linear load is initially 75° . The firing angle of the controlled rectifier is changed suddenly at 0.15s to 60° . At 0.25s, the firing angle is changed once more to 45° . The Phase a supply and load currents are shown in Fig. 13(a) and Fig. 13(b), respectively. It is clear for Fig. 13(a) that before activating the APF, the supply current was highly distorted. However, after the APF activation, the supply current becomes almost sinusoidal even at the instants of the dynamic changes. The THD of the supply current is reduced from 33% to less than 5%. The dc-side voltage is shown in Fig. 13(c). At each sudden load increase, a dip in the dc voltage occurs with duration less than two power cycles and depth less than 5%. The voltages across the two dc-side capacitors are illustrated in Fig. 13(d) and Fig. 13(e). Fast dynamic performance without overshoot and tight dc-side voltage regulation and NP compensation, of the proposed APF control methodology, are evident from these results.

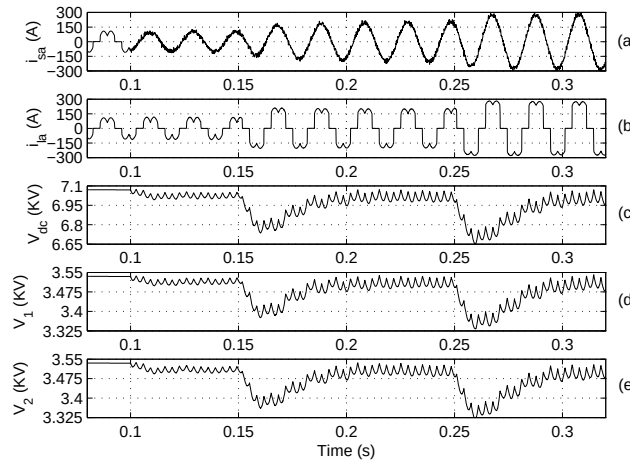


Fig. 13 Dynamic performance: (a) load current, (b) supply current, (c) dc-side voltage, (d) voltage across C_1 , and (e) voltage across C_2

C. Case 3: FC-Based APF to Compensate for Medium Voltage Controlled Rectifier Load

In this case, the performance of the proposed APF based on FC inverter is examined by compensating the harmonics generated from a controlled rectifier operating at the same firing angles of the previous case. The circuit parameters of the FC-based APF, shown in Fig. 2, are given in Appendix B and the clamping capacitors, C_3 , are $50\mu\text{F}$. The APF is activated at 0.1s. Fig. 14(a) portrays the ac supply current for phase a and the load current is illustrated in Fig. 14(b). It is clear that the proposed FC-based APF compensates the harmonics in the load current successfully allowing in such way for a sinusoidal supply current. The THD of the supply current is decreased to less than 5%. The dc-side voltage is shown in Fig. 14(c). The proposed control algorithm regulates the dc-side voltage at its desired value with fast dynamics even when the load is changed. Finally, Fig. 14(e) indicates the clamping capacitor voltage compared to half the dc-side voltage. Once the APC is activated, the clamping

capacitors are started to charge until its voltage v_{c3} achieve $v_{dc}/2$. It is obvious that the clamping capacitor voltage is tightly maintained at half the dc -side voltage through the choice between the appropriate redundant zero-switching states given in Table II. It is noteworthy that during the initial charging period of the clamping capacitors, the proposed FC-based APF succeeds in compensating the load harmonics.

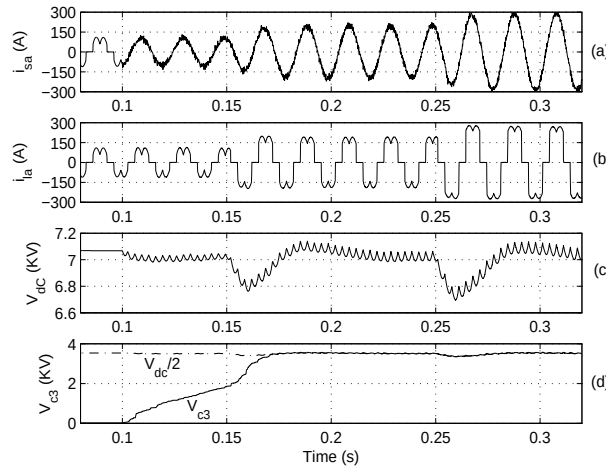


Fig. 14 Study case 3: (a) phase a supply current, (b) phase a load current, (c) dc -side voltage, and (d) clamping capacitor voltage compared to $v_{dc}/2$

VI. CONCLUSIONS

This paper presents a simplified control algorithm for the shunt APF based on clamped-type (NPC and FC) multilevel inverters. The ADALINE algorithm is used to adaptively track the load harmonics. With the aid of simple PI controllers, the necessary reference current components for regulating and balancing the voltages across the dc -side capacitors of the NPC inverter are synthesized. Another important feature of the proposed control algorithm is the possibility to apply it to the FC-based APF. Furthermore, the dual band HCC is easily adapted to allow for the clamping capacitor voltage balancing as a part of the current control. Different study cases are conducted to evaluate the performance of the proposed APF based on clamped-type multilevel inverters using PSCAD/EMTDC software package. The capabilities of the proposed control algorithm to track the load harmonics, to regulate the dc -side voltage, and either to compensate the NP potential for the NPC inverter or to maintain the voltage across the clamping capacitors of the FC inverter are verified and demonstrated with different nonlinear loads. Fast dynamic performance, accurate harmonics tracking and tight dc -side voltage regulation of the proposed control algorithm are revealed from the simulation results.

APPENDIX A

$v_{sa}, v_{sb},$ and $v_{sc}=380$ v, $f_o=50$ Hz, $R_{sa}, R_{sb},$ and $R_{sc}=2\text{m}\Omega$, $L_{sa}, L_{sb},$ and $L_{sc}=0.01\text{mH}$, $L_a, L_b,$ and $L_c=0.4\text{mH}$, $R_{load}=1.5\Omega$ to 3.5Ω , $L_{load}=35\text{mH}$, C_1 and $C_2=1000\mu\text{F}$, $V_{dc}^*=900$ v.

APPENDIX B

$v_{sa}, v_{sb},$ and $v_{sc}=3000$ v, $f_o=50$ Hz, $R_{sa}, R_{sb},$ and $R_{sc}=2\text{m}\Omega$, $L_{sa}, L_{sb},$ and $L_{sc}=2\text{mH}$, $L_a, L_b,$ and $L_c=1\text{mH}$, $R_{load}=10\Omega$, $L_{load}=30\text{mH}$, C_1 and $C_2=1000\mu\text{F}$, $V_{dc}^*=7000$ v.

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